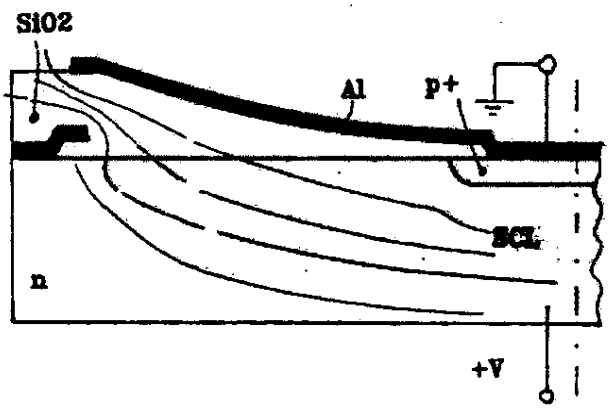

Fig. 1 Basic planar p-n junction using field plate

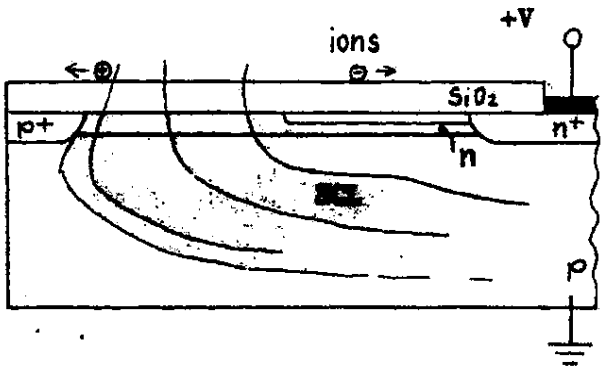

Fig. 3 "Resurf" junction termination

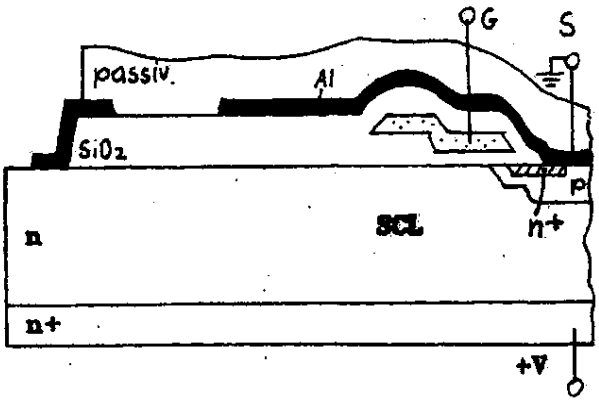

Fig. 2 Junction termination of a V DIMOS FET

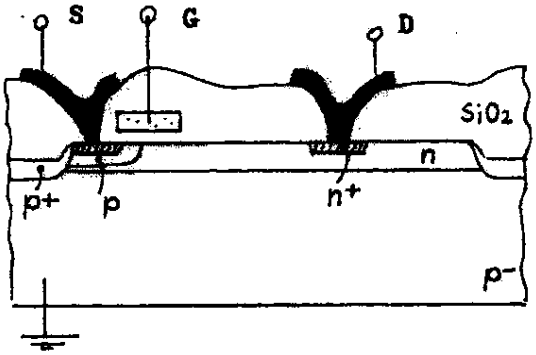

Fig. 4 Resurf-based lateral HV MOSFET

The other method of surface field reduction is the "Resurf" principle (1) shown in its simplest form in Fig. 3. The heavily doped region is surrounded by a lightly doped surface layer, which terminates in a heavily doped region of the substrate. The weakly doped surface layer depletes, compensating for the substrate space charge under reverse bias and causing a forced lateral extension of the surface space charge region. As a result, the surface field becomes virtually constant, having only small peaks at the two ends of the lightly doped zone.

The Resurf principle, although compatible with most IC processes, particularly those using ion implantation, is used mainly for lateral HV MOS devices. Different implementations exist which deviate slightly from the basic structure, as illustrated in Fig. 4.

INTEGRATED DEVICES

Two main groups of ICs can be distinguished in the integration of HV structures.

The HV ICs integrate generally low voltage logic and HV output stages on a single chip. They are devoted mainly display driving and telephone IC applications where the essential performance factor is high voltage capability.

The other group contains chips with integrated low voltage input circuit or functionally integrated structures.

These devices are used to switch really high power and are supported by additional functions to achieve superior performance.

HV ICs

The HV ICs can be classified according to the isolation techniques used.

Junction isolation is the oldest isolation form and has been used widely by bipolar IC producers. A novel version working at up to 200 V has been in-

troduced by Stanford University (2). Recent versions have been developed by TI (3, 4) by Thomson CSF (5) and by Motorola (6) for its "smart power" products. A junction-isolated HV DMOS device is shown in Fig. 5.

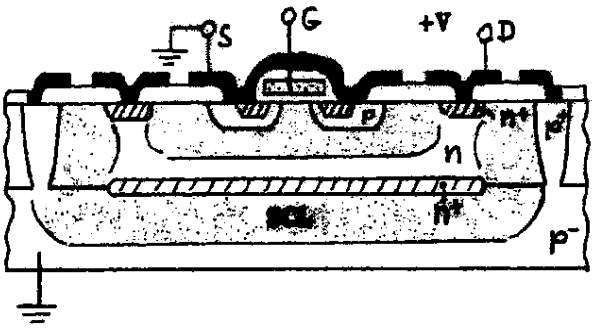

Fig. 5 Junction-isolated HV MOSFET

The device region is separated from the rest of the IC by deep p-diffused walls. Both drain and source can have a positive voltage. The drain-substrate and drain-source junctions are terminated by field plates. For interconnections two-layer Al-metalization can be used. Technological restrictions limit the voltage range of junction-isolated HV devices to about 200 V. The flexibility of the junction isolation is demonstrated by the TI technology, which is capable of integrating HV DMOS and HV bipolar transistors with low voltage n and p-channel MOSFETs and bipolar transistors.

Dielectric isolation is the most obvious form, using a real insulating layer to prevent interactions between IC parts. Each individual HV device is located in an insulated tub and behaves like a discrete component, and can be biased independently from another device and from the substrate (see Fig. 6). Dielectric isolation seems to be eminently suitable for telecommunications circuits, due to its free biasing capability. Bell Labs has developed a unique 500-V gated diode crosspoint array, and can also fabricate vertical DMOS FETs in a tub (7, 8). Hitachi and NTT (9) use 350-V n^- and p^+ gate-fired thyristors, and gate turn-off thyristors in their telecommunications circuits. All dielectrically isolated HV devices have a simple field plated-junction termination.

Technologically interesting is the spinel-isolated version which has been presented by Fujitsu (10), which seems to make use of a technology simpler than the normal DI technique.

The Silicon-on-sapphire (SOS) technique for HV ICs was demonstrated recently in some new developments. The offset gate devices mainly used are essentially special versions of the Resurf structure. Fig. 7 shows a typical n-channel high-voltage MOSFET which has been presented by Nippon E. Co (11). The device achieves 1000 V V_{BR} with a 100 /um-long drift region. Data is not available on the stability of the electrical characteristics. Similar devices have been used for a 500-V CMOS SOS pulse generator.

Lateral HV MOS FETs in ICs are especially suitable for display driving. Different approaches presented recently have come from Xerox (12), Tektronix (13), Sharp (14) and Siemens (15). All of these manufacturers have been able to integrate conventional n-MOS low-voltage logic with high-voltage output-transistor stages; however, all but the Siemens solution are open-drain high voltage devices with a ring-shaped source surrounding the drain.

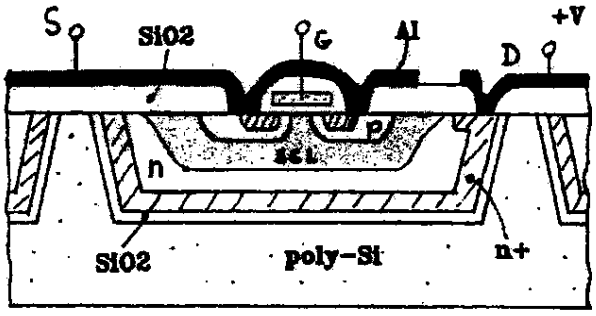

Fig. 6 Dielectric isolation of a V-DMOS FET

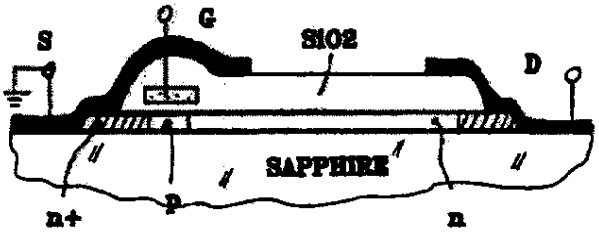

Fig. 7 SOS HV MOSFET

The HV DIMOS device developed by Siemens is shown schematically in Fig. 8 in conjunction with the integrated low-voltage n-MOS depletion load inverter. The HV isolation is provided by a polysilicon shield. The drift region is V-shaped to avoid carrier multiplication under current flow. The Tektronix solution achieves the same results by using two-step implantation in the drift region. One disadvantage of the lateral HV MOS circuits is the large area of the HV devices. The drift region must be about 15 /um in length per 100 V of drain voltage, and the open drains need large bonding pad areas.

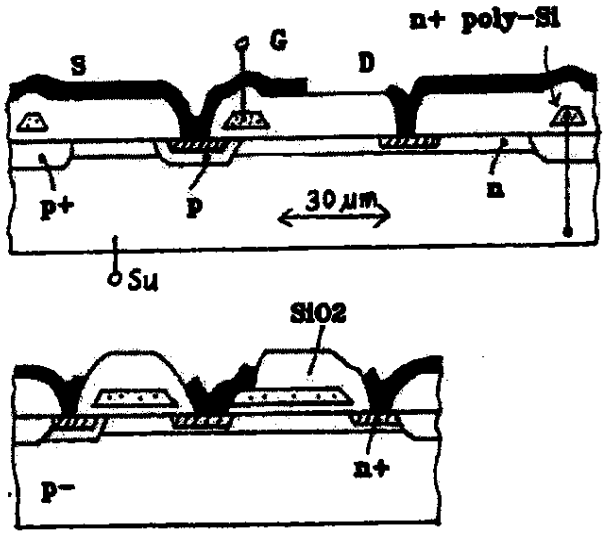

Fig. 8 Lateral HV MOSFET and integrated low-voltage inverter

Comparison of HV-IC Techniques

From an economical point of view, the junction-isolated and the lateral HV MOS solutions are the most attractive solutions, being compatible with well-established IC processes. However, they use a relatively large portion of the area for isolation between the components and for the HV devices. The SOS technique offers good isolation between the devices, but SOS HV MOSFETs have the same drift region as the bulk silicon devices, and SOS packing density is practically the twice of lateral HV MOS ICs. The dielectric isolation technique seems to be the most promising. It allows the highest packing density, because of the devices used even the MOSFETs can be made in vertical versions, and the area of the isolation is minimal. DI devices operate on independent potentials.

It can be predicted that lateral MOS ICs are likely to be used in the future for display driving, while the high-performance HV ICs for telecommunications will continue to be fabricated by dielectric isolation. The junction isolation is most likely to be used for voltages of up to 200 V.

Integration of Power Devices

Old-fashioned power devices employ a technology which has become increasingly unable to support higher integration levels. New possibilities have been raised recently with the introduction of IC fabrication and design methods for vertical DMOS FETs. These are essentially highly complex ICs. The motivation to search for new devices based on IC techniques is based on the fact that, although the MOS power devices have superior speed, current and input power performance, their on-resistance in the high-voltage range is worse than that of bipolar thyristors or transistors with the same area. There are some interesting approaches which allow bipolar current-carrying capability to be combined with MOS performance.

BI-MOS (16, 17) covers a structure consisting of a vertical DMOS FET and bipolar power transistor having common drain and collector on a chip. The two integrated power devices can be connected in parallel, resulting in a low on-resistance when properly triggered, or they can be adjusted in a Darlington configuration which at the same time offers MOS input resistance and low on-resistance.

MOSFET thyristors are combined, functionally integrated devices (18). Their structure is shown in Fig. 9. It produces high input resistance, excellent dv/dt and superior di/dt capability. The first commercial type was introduced by Motorola recently.

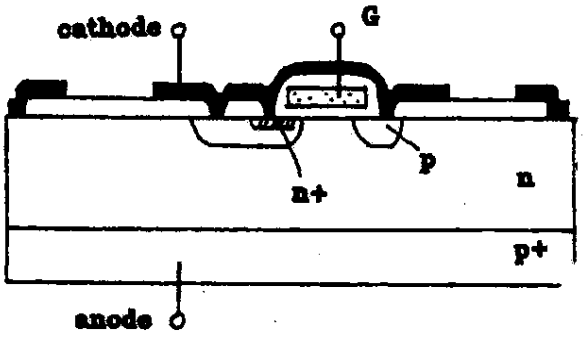

Fig. 9 MOS thyristor

The idea of opto thyristors and triacs was obvious: a FET-controlled thyristor needs only a small amount of charge to bias the MOS gate and turn the thyristor on; this charge can be supplied by a relatively insensitive and simple integrated photodetector. The idea has been implemented in vertical and lateral thyristors and triacs (19).

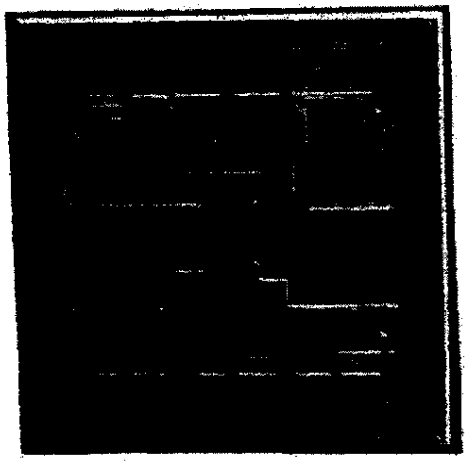

Fig. 10 Lateral MOS opto triac

Fig. 10 shows a lateral triac which blocks 600 V, carries 0,3 A and has excellent dv/dt. Furthermore, the LED current for triggering the DIP 6-packaged device is only 1 mA. The integrated circuitry of the device consists of enhancement- and depletion-type lateral MOSFETs, bipolar phototransistors, vertical MOSFETs and two anti-parallel connected lateral thyristor devices. The junction termination is solved by a combination of field plates and conductive amorphous silicon coverage. Opto-FET-thyristors are also feasible in vertical form for higher currents and higher voltages, where they will be used as firing devices for large power thyristors.

The static induction transistor (SIT) (21) and the field controlled thyristor (FCT) are complex devices, integrating inherently an FET and a bipolar transistor or thyristor. In their normal mode (with reverse gate bias) they operate like junction FETs with very short channels, but act as bipolar devices at forward gate bias. Their high working speed is an attractive property. A very interesting switch combining the MOSFET and the FCT was presented recently (20). It is a very promising structure for high power switching, e. g. AC motor drive.

Future developments

Integration of a vertical power MOSFET with low voltage control circuity is highly feasible and is likely to occur in the near future. The name "smart FET" for such a device is already in common use. The simplest form will be perhaps a MOSFET with an n-channel depletion-load IC in its p "body" region. Its preferred application will be in switch-mode power supplies or in automotive electronics.

In contrast to the integration of a power device with a logic IC, the feasibility of integrating more independent vertical devices (e. g. power FETs on one chip) seems to be unlikely. A kind of power-dielectric-isolation would be needed.

The MOS-based optothyristors will develop rapidly to accommodate higher voltages and currents. This will also give impetus to the development of the high-voltage planar p-n junction technique. High-sensitivity optothyristors for 1500 - 3000 V are likely to appear in the next two years.

Another device type which will benefit from the breakthrough of IC fabrication methods for power integration is the GTO family. Gated turn-off thyristors are easier to manufacture using the fine-resolution vertical MOS technology than with the older methods. The FCT-MOSFET combination suggested by Baliga (20) seems also to be a subject for integration.

CONCLUSION

High voltage ICs compatible with established fabrication techniques have recently become feasible. There is, however, no optimum solution: the different approaches are suited to specific applications. The most flexible HV IC technique seems to be dielectric isolation.

Integration with respect to high-voltage, high-current devices has been supported by the development of vertical MOSFETs. New power chips consisting of a power device and a logic circuit (smart FET, optothyristor, triac, BI-MOS, FCT-FET) are highly feasible, but the integration of more than one independent power device on the single chip seems highly unlikely.

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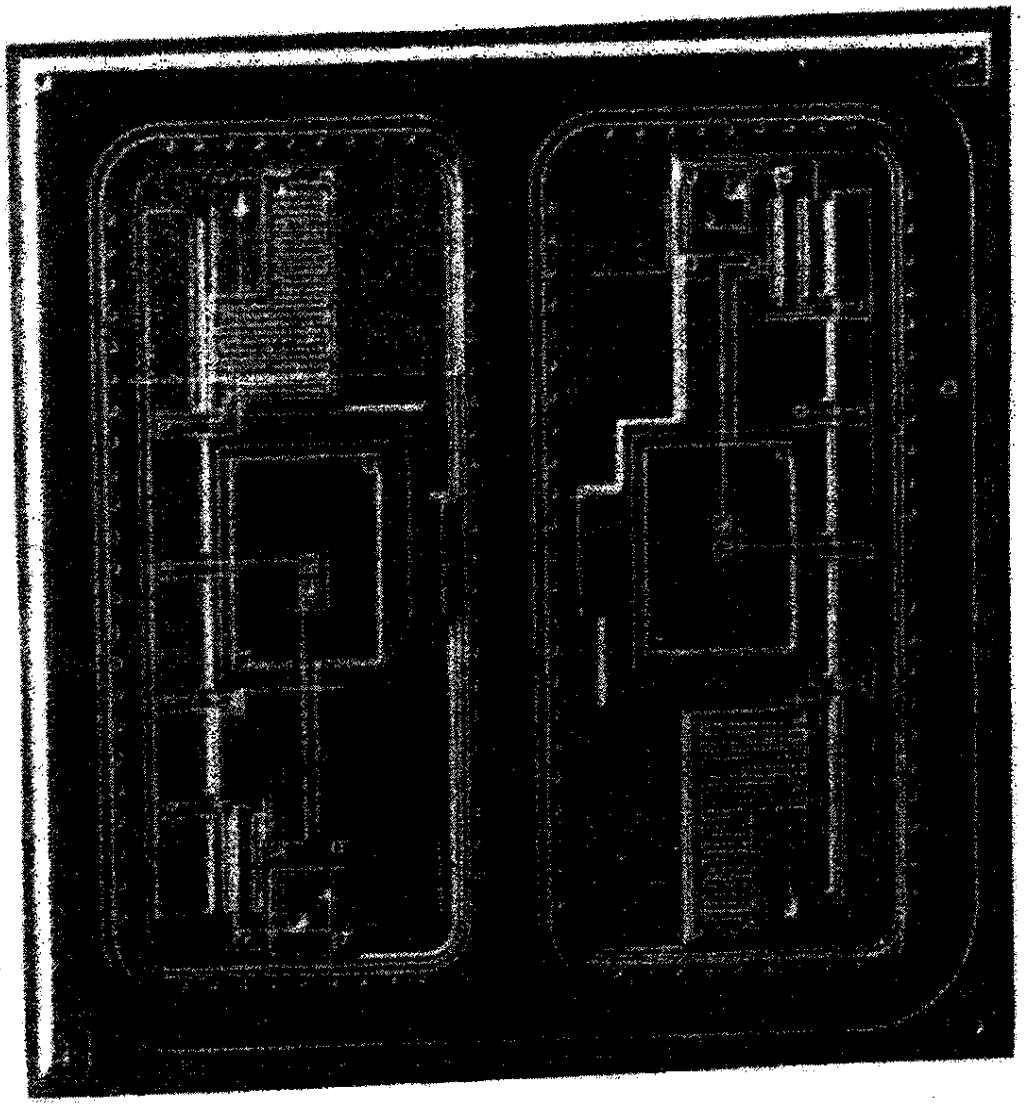

Fig. 10 Lateral MOS opto triac

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High-Voltage DIMOS Driver Circuit

MICHAEL POMPER, LUDWIG LEIPOLD, JENŐ TIHANYI, AND HANS-EBERHARD LONGO

Abstract—**High-voltage output driver circuits realized with double-implanted MOS (DIMOS) transistors are presented. Breakdown voltages exceed 100 V. Dynamic bootstrap techniques resulted in circuits combining low power (5 mW) and fast switching times (150 ns) at typical operating conditions of 5 V/50 V, 50 pF, and 16 kHz.**

INTRODUCTION

There is a great interest in integrated circuits, especially in MOS circuits, with part of the circuit operating at high voltages, because board area and system costs can be reduced markedly. So far CMOS combined with double-diffused MOS (DMOS) transistors [1], silicon on sapphire [2], and diffused self-aligned (DSA) MOS techniques [3] have been used for this purpose. The technique presented here combines high-performance 5 V n-channel E/D logic circuits in DIMOS-technology [4] with high-voltage transistors. The integration of these two types on a single chip requires only one additional process step.

DIMOS STRUCTURE

DMOS or DSA transistors with their short channel length and their asymmetric structure are suited to achieve a high transconductance as well as a high breakdown voltage. The double-implanted or DIMOS device has physically the same structure and shows a similar behavior. An additional advantage of the DIMOS transistor, however, is its ease of fabrication. Doping and active channel length can be tightly controlled by ion implantation.

Fig. 1 shows a "low-voltage" DIMOS device with its typically beveled polysilicon gate (ramp gate) and the submicron-channel, fabricated in a standard LOCOS process. The enhancement-type short DIMOS-channel with a length smaller than 0.5 μm is determined by the ramp angle of the polysilicon gate and the boron implantation (typical 2.0×10^{12} cm^{-2}; 150 keV). This implantation is masked at the drain edge, determines the DIMOS channel, and controls the threshold voltage. The geometrical channel length of this device including the depletion-type long channel is typically 5 μm. Table I shows the most important process, device, and circuit characteristics of the DIMOS technology. Typical breakdown voltages of the turned-on transistor are about 12 V.

HIGH-VOLTAGE TRANSISTORS

Spacing the gate from the n^+-drain region and extending the n-type depletion region to the drain results in a high-voltage device (Fig. 2). This drift region with the length L_D, which acts like a pinch resistor, is made with the same phosphorus implantation step as the depletion channel (typical 1×10^{12} cm^{-2}; 120 keV). A high voltage on the drain can now drop along the pinch resistor. For the fabrication of these transistors one additional masking step is necessary. Thereby the drift region has to be masked during the high-dose source/drain implantation. A drawback of this structure is an increased on-resistance. A typical value of the pinch resistor is 7 kΩ/□.

Transistors with a ring-shaped gate surrounding the n^+-source region and with spacings between the active device and the p^+-doped field regions (Fig. 2) have the following high-voltage capabilities:

1) drain versus source and gate, respectively;
2) drain, gate, and source, respectively, versus the substrate.

Therefore a high-voltage restriction exists only between the gate and source terminals (gate oxide breakdown ≥ 25 V), which must be taken into account in the circuit design. Aluminum field plates at the drain and gate edges increase the breakdown voltage additionally. Field inversion can be avoided by grounded polysilicon field plates.

Fig. 3 shows the current-voltage characteristics of two devices with different drift region lengths L_D. Typical breakdown voltages of more than 100 V are achieved if $L_D = 12$ μm [Fig. 3(a)]. This device type has been used to design the high-voltage output buffers. If L_D is enlarged, the breakdown voltage can be increased to a value where the bulk breakdown

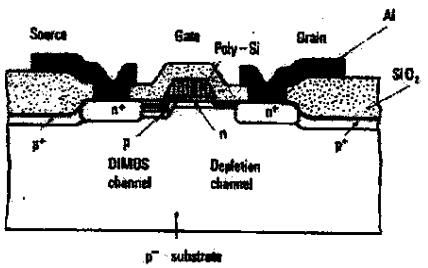

Fig. 1. Cross section of a DIMOS transistor.

TABLE I
DIMOS-PROCESS, DEVICE, AND CIRCUIT CHARACTERISTICS

SUBSTRATE DOPING	(TYP.)	20 Ω·cm
GATE OXIDE THICKNESS		65 nm
LITHOGRAPHY	(MIN)	5 μm
THRESHOLD VOLTAGE	(TYP)	0.5 V
TRANSCONDUCTANCE	(MAX)	25 mS/mm
GATE DELAY	(TYP)	5 ns
	(MIN)	1 ns
POWER DELAY PRODUCT	(TYP)	2.5 pJ

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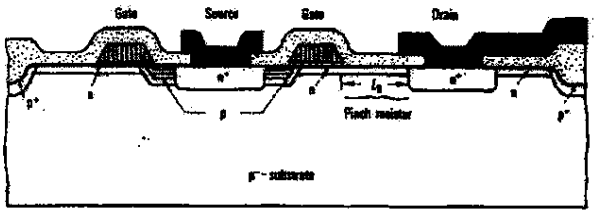

Fig. 2. Cross section of a high-voltage DIMOS transistor.

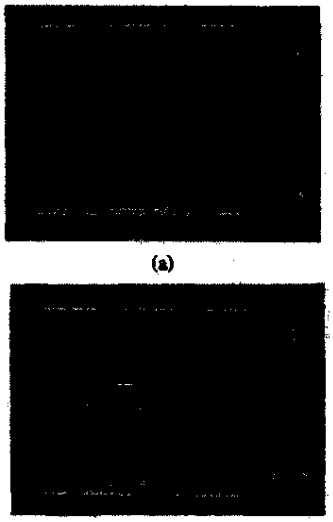

Fig. 3. Current-voltage characteristics of high-voltage transistors: (a) $L_D = 12\ \mu m$; $BV_{DS} > 100$ V; (b) $L_D = 30\ \mu m$; $BV_{DS} > 200$ V.

occurs. A 30 μm-test device can handle more than 200 V [Fig. 3(b)]. With higher substrate resistivities, for example 50 $\Omega \cdot$ cm, breakdown voltage is improved to about 300 V. Compared with DMOS the DIMOS device shows a different punch-through behavior. The reason is that the p-doped DIMOS channel with its relative high concentration surrounds the n⁺-source region only in lateral, but not in vertical (bulk) direction (Fig. 2). Thus at low substrate dopings punch-through can occur earlier than in DMOS devices. Therefore a more sophisticated layout of DIMOS devices must be employed.

Another important point to consider in circuit design is the bulk effect. If these transistors are used in a high-voltage push–pull configuration, the pull-up device suffers severely from an increasing threshold voltage.

Fig. 4 shows the threshold voltage behavior at high substrate bias voltages. Four typical curves are plotted in this diagram. Parameters are the substrate resistivity with 20, 50, and 80 $\Omega \cdot$ cm and the boron implantation dose for the DIMOS channel with 2 and 2.5 X 10^{12} cm^{-2}, respectively. These curves show, that for operating voltages in the range of 100 V and more, a substrate resistivity of more than 50 $\Omega \cdot$ cm should be used. Then an efficient circuit operation with threshold voltages below 2.5 V seems to be possible.

High-Voltage Output Buffer

Our first design was the well-known single-stage output buffer circuit with a bootstrap push–pull configuration [5], shown in Fig. 5.

Three high-voltage devices—T_1, T_2, and T_3— are necessary, further, the bootstrap capacitor C_B and the protection device

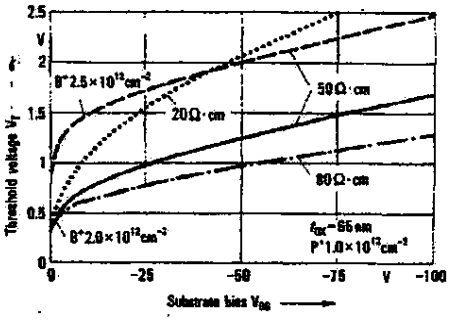

Fig. 4. Threshold voltage (V_T) behavior at high substrate bias voltages V_{BS}. Parameters: substrate resistivity; boron dose of the DIMOS channel implantation.

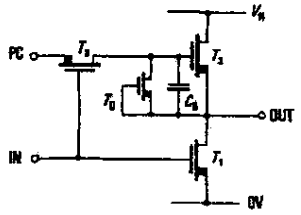

Fig. 5. Circuit diagram of the single-stage output buffer circuit.

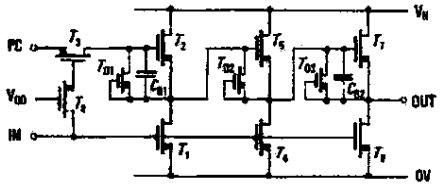

Fig. 6. Circuit diagram of the three-stage output buffer circuit.

T_D. This device is designed as a low-voltage transistor with a breakdown voltage below 25 V, which prevents the pull-up device T_2 from a gate oxide breakdown.

For a pull-up operation, first the bootstrap capacitor C_B is charged via the switched-on transfer device T_3 with the precharge signal *PC* going "high." When the slightly delayed (~20 ns) input signal IN goes "low," T_3 is switched off. Thus the gate of the pull-up device T_2 is isolated and can be bootstrapped to a voltage level well above V_H.

The circuit must be able to operate with 5 V input and precharge levels. To achieve both high switching speed and low power dissipation, the following provisions should be made.

1) High-voltage dc paths to ground are not allowed. Therefore usual level shifters cannot be used.
2) The precharge time should be minimal.
3) The effective gate voltage of the pull-up device should be large enough to compensate for stray capacitors—and the bulk effect.

The last point cannot be accomplished by this circuit. Therefore it suffers from a large rise time at higher supply voltages. Applying 50 V rise times of more than 1 μs have been measured. A better solution is a three-stage output buffer design shown in Fig. 6. The first stage is constructed similarly to the single-stage circuit. The additional transistor T_8 effects a bootstrapping of the gate of the transfer device T_3. Thus the full supply voltage level V_{DD} is applied to the bootstrap capacitor C_{B1} during precharge. The second stage with T_4 and T_5 serves as buffer between the first stage and the bootstrap output stage with T_6, T_7, and C_{B2}.

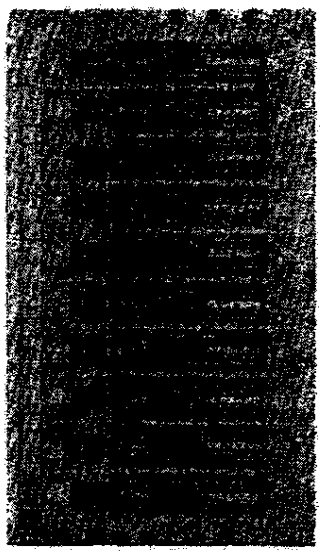

Fig. 7. Microphotograph of a test circuit with 10 output buffers.

The main advantage of this design is the possibility of applying higher effective voltage levels to the pull-up output device T_7. This results in markedly reduced rise times. Furthermore power dissipation during precharge is lowered, because the first stage can be designed very small. An additional advantage is a full voltage swing at the output—independent of the high level achieved by the first stage. Finally the rise time behavior is less sensitive to higher load capacitances.

Experimental Results

A test chip with ten three-stage output buffers, shown in Fig. 7, has been used for the experiments. The circuit was designed for an operation up to 60 V. The output devices have a channel width of 300 μm and a current carrying capability of about 25 mA. One buffer occupies a die area of 0.25 mm^2.

Typical operating conditions are: supply voltage $V_{DD} = 5$ V; $V_H = 50$ V; the frequency $f = 16$ kHz, and the load capacitance $C_L = 50$ pF. The measured waveforms in Fig. 8 show the 5 V-input pulse and the output voltage. Rise and fall times are less than 150 ns. Power dissipation of the high-voltage circuit part is about 2.5 mW. An additional power of 2 mW is dissipated by the input delay and buffer circuit.

A certain drawback of the three-stage circuit configuration is that the switching behavior is worse if the capacitive output load is too small. This is effected by a too fast switching output stage coupled with an insufficient precharge. The result is a reduced high-output level. Therefore the following rule for dimensioning the time constants τ of the different stages for pull-up must be considered:

$$\tau_{\text{stage 1}} < \tau_{\text{stage 2}} < \tau_{\text{stage 3}}. \quad (1)$$

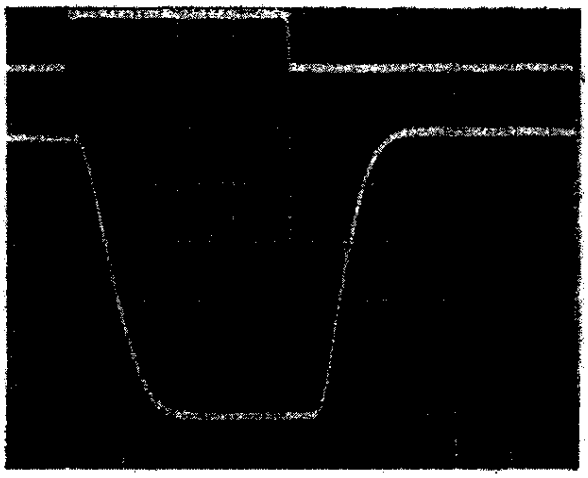

Fig. 8. Measured voltage waveforms ($V_H = 50$ V; $C_L = 50$ pF); upper trace: input voltage (5 V/div); lower trace: output voltage (10 V/div); time 100 ns/div.

The leakage currents of the high-voltage devices are similar to those of the low-voltage transistors. Minimum operation frequencies at room temperature are in the range of 1 Hz.

Conclusions

A technological and design method has been described: how high-voltage circuit parts can be simply involved in DIMOS n-channel silicon gate E/D circuits. The results show that it should be possible to realize circuits operating in a voltage range up to 300 V, if some technological parameters, for example, substrate doping and the isolation oxide thickness, and device geometry are optimized.

The fields of applications for these circuits are display- and piezo-drivers as well as any high-voltage analog and digital functions.

Acknowledgment

The authors wish to thank G. Lindert and his group for design assistance and G. Plasa and his group for circuit fabrication.

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End of Special Section

DX 622

INTEGRATED HIGH AND LOW VOLTAGE CMOS TECHNOLOGY

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ABSTRACT

Novel, complementary high- and low-voltage MOS transistors are described. The high-voltage CMOS transistors were designed and fabricated using the same shallow well as that of low-voltage CMOS transistors, thus enabling integration of the devices without the use of dielectric isolation. The high voltage p-channel transistor is built inside of the n-type well and the p-type offset channel is used to separate the drain area from the gate, which has the same oxide thickness and threshold voltage as a low-voltage p-channel transistor. The high-voltage n-channel devices are built in the high resistivity p-type substrate, using an n-type offset channel to separate the N^+-drain and the gate. The high- and low-voltage CMOS transistors were fabricated using 55-75 ohmcm, p-type substrate with a minimum channel length of 8 microns for the high-voltage and 3 microns for the low-voltage transistors. Drain to source breakdown voltages above 250V and above 23V have been demonstrated for the high-voltage and low-voltage transistors respectively.

INTRODUCTION

High-voltage integrated transistors have found various applications as analog and switching devices. The integrated high-voltage and low-voltage CMOS technology offers circuit performance advantages over N-channel technology in terms of power dissipation and speed, and also offers some additional flexibility in circuit design unavailable otherwise. Several efforts have been made to develop an integrated high- and low-voltage CMOS technology (1-3). A high- and low-voltage SOS/CMOS technology has been described in (1). Integrated bulk silicon CMOS devices (2,3) have been fabricated by utilizing deep impurity diffusion which creates isolated wells of opposite dopant to the substrate. The drain depletion region in such a design expands vertically and the breakdown voltage is thus limited by the depth of the diffused well.

In this paper a shallow well concept is described for the fabrication of high- and low-voltage CMOS transistors in bulk silicon. The p-channel high-voltage transistors are built inside an identical well as that for the low-voltage transistors. The vertical expansion of the depletion region is transformed into horizontal expansion by utilizing the offset channel, which is in turn depleted prior to the gate oxide breakdown. A depleted region, free of carriers, supports high, drain-to-source breakdown voltage. The high-voltage n-channel transistors are built in the high resistivity p-type substrate, utilizing the offset channel to provide high drain-to-source breakdown voltage. The low-voltage p- and n-channel transistors have the same gate oxide thickness and threshold voltage as the high voltage transistors.

DEVICE STRUCTURE

The high-voltage p- and n-channel transistors have an enclosed circular structure with the drain in the center of the device. The p-channel devices are built inside of an n-well, which is about 5 microns deep. The well has a polysilicon field plate to enhance the well to substrate breakdown voltage. The n-channel transistors are built in the high resistivity p-type substrate. The heavily doped drain area is separated from the gate by an offset channel, Figure 1. When the transistors are turned on, current flows from source through the gate channel and the offset, low-doped channel to the drain as it does in a conventional MOS transistor. When the devices are turned off and the voltage is applied between source and drain the p- and n-channel transistors behave somewhat differently. In the p-channel transistor, the offset channel depletes and simultaneously depletes the well underneath. The entire well region between drain and gate becomes depleted at a certain voltage below the gate-oxide rupture voltage, and any additionally applied voltage then drops across that region, which then behaves as an insulator. When the well and offset channel are totally depleted the electric field becomes largely horizontal and the device must be treated as a two-dimensional structure. The simulations show that the maximum horizontal electric field is a function of the doping level in the offset channel and well and is sensitive to the charge mismatch between them. In the n-channel transistor during turn-off, the offset channel and the region of the substrate underneath is depleted providing a region free of carriers, which then supports high drain voltage.

The low-voltage n- and p-channel transistors are self aligned to their gates.

FABRICATION PROCESS

The fabrication process developed for an integrated high- and low-voltage CMOS transistor has 11 masking steps and utilizes (100) oriented, 55-75 ohmcm resistivity, p-type silicon.

The initial oxide film is grown and the wafers are patterned for the well. Phosphorus is implanted, driven at high temperature to a depth of 5 microns and then the

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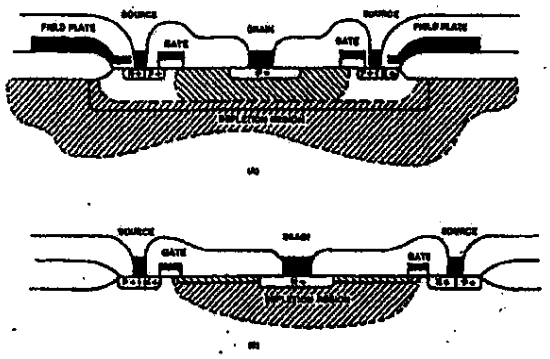

Figure 1. (a) High voltage p-channel structure; (b) High voltage n-channel structure.

wafers are oxidized. An Si_3N_4 film is deposited and patterned, followed by patterning and implanting with boron for the channel stop areas. A thick oxide is grown selectively in the field area. Then the Si_3N_4 film and the initial oxide underneath is removed and the gate oxide of 1000 Å thick is grown. The threshold voltage of the n-channel transistors is adjusted by patterning and implanting boron in the gate areas. The polysilicon film is deposited, doped, patterned and etched. The p-type offset channel is formed by implanting boron followed by patterning and implanting phosphorus for the n-type offset channel. The heavily doped P^+-source and drain areas are formed by implanting BF_2 into photoresist patterned wafers. Then the thin oxide film is grown to protect implanted areas and the new photoresist pattern is printed and etched for the N^+ source and drain. The N^+ areas are formed either by As-implant or by outdiffusion from the phosphorus rich CVD SiO_2 film which is deposited and reflowed at high temperature. Contacts are etched and the interconnections are formed by patterning an Al film. The protective phosphorus-doped SiO_2 film is deposited and pad areas are defined.

EXPERIMENTAL RESULTS

In this series of the experiments for the development of the integrated high- and low-voltage CMOS transistors the shallow well concept was verified. Although the reported results are satisfactory for the purpose for which they have been developed, it is expected that higher breakdown voltages can be achieved by further optimising the process parameters.

The typical drain characteristics of the high-voltage n-channel transistors are shown in Figure 2. The drain breakdown voltage at zero biased gate is in excess of 400V, exhibiting almost linear dependence on the offset channel length. The drain leakage current is less than 1 nA. The typical characteristics of the p-channel transistors are shown in Figure 3, when the drain is connected to the substrate and the source is connected to the field plate. The drain breakdown voltage is over 225V, and the drain leakage current is less than 1 nA at zero gate bias voltage. The well-to-substrate breakdown voltage is in excess of 400V for the 30-micron wide field plate. Both high-voltage transistors are stable at high temperature. Punch-through between source and drain is not observed for channel gate lengths as small as 8 microns.

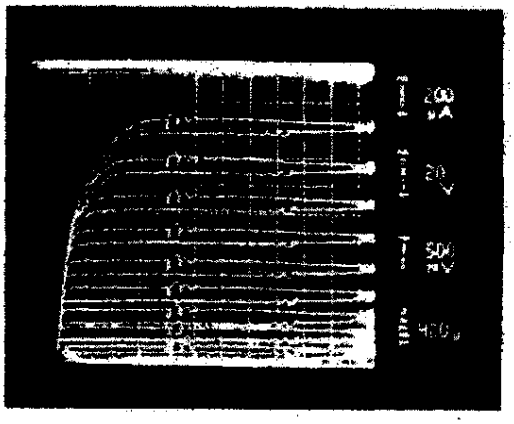

Figure 2. Typical drain characteristics of high-voltage p-channel device with the offset channel 40 microns long.

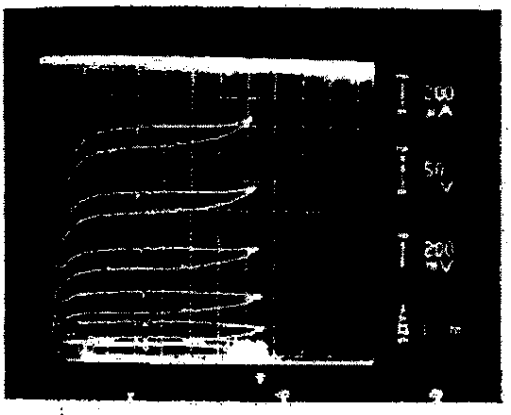

Figure 3. Typical drain characteristics of high-voltage n-channel device with the offset channel 70 microns long.

The low-voltage p- and n-channel transistors as well as the high-voltage transistors have a threshold voltage of -2.5V and +1V respectively. The typical drain characteristics of low-voltage p- and n-channel transistors of 50 x 50 microns are shown in Figures 4 and 5. The non-symmetrical values of the threshold voltage for the p- and n-channel transistors are dictated by the specific circuit requirements. The drain breakdown voltage at zero gate-to-source voltage exceeds 25V for both types of transistors. The short channel affects such as source to drain punch-through and the threshold voltage changes are depicted in Figures 6 and 7. The threshold voltage changes are small for the p-channel transistors with channel length as small as 2 microns. However, the n-channel transistors have more pronounced changes of the device parameters at much longer channels due to the high resistivity substrate. The short channel effect is significantly reduced in the experiments with the "twin tub" process (curve 3), when the second p-type tub is diffused in the area of the n-channel transistors and the impurity concentration is higher than in the substrate.

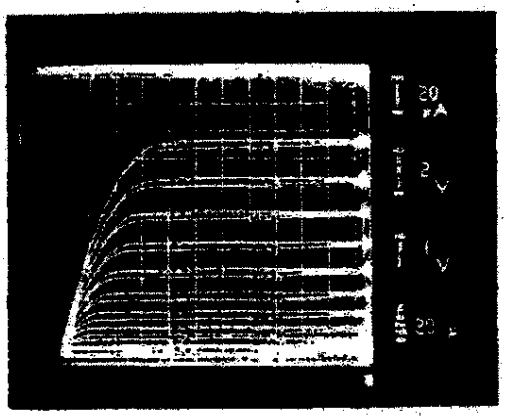

Figure 4. Typical drain characteristics of low-voltage p-channel device.

Although the SCR-type of trigger (latch-up) between different circuit components has not been completely eliminated, the regenerative effect was noticeably suppressed by shorting the sources of the devices to the silicon underneath and the SCR-type of latch-up was not observed, in the operating current range.

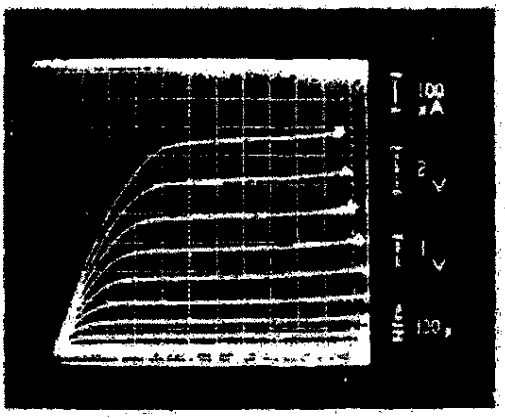

Figure 5. Typical drain characteristics of low-voltage n-channel device.

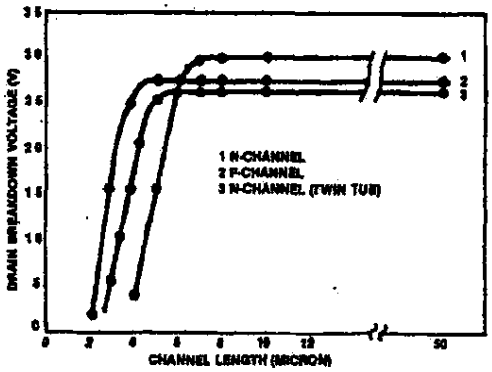

Figure 6. The source to drain breakdown voltage vs. channel length.

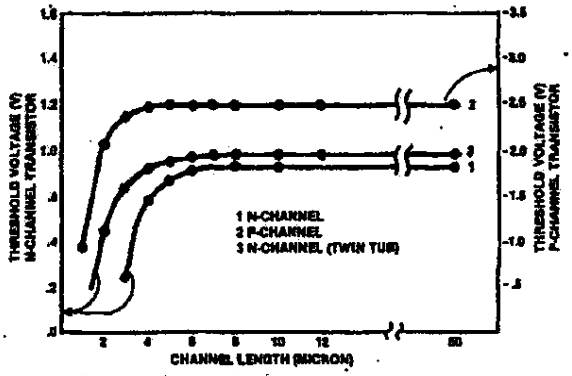

Figure 7. The threshold voltage vs. channel length.

CONCLUSION

A new concept of the integrated high- and low-voltage CMOS transistors has been developed and verified. High-voltage transistors of a circular geometry are built in a high resistivity substrate together with low-voltage transistors. The blocking capabilities of the high-voltage transistors are in excess of 250V and show stable operation at high temperature.

ACKNOWLEDGEMENTS

The authors are grateful to all of the people at Xerox Microelectronics Center, who contributed to this project and special thanks to Joan Hack for her wafer processing effort.

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DX 623

SESSION II: CONSUMER CIRCUITS

WAM 2.3: Integrated High-Voltage Video Amplifier for Color TV

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THE COLOR TV cathodic tube is driven by a high voltage, wide-band, low switching time dc amplifier. Hybrid and discrete amplifiers are used in present TV receivers. The integration of this function requires a high voltage capability for the circuit to obtain correct output signal dc level (brightness) and dynamic range (contrast). The presence of high voltage in an integrated circuit can induce parasitic channels in the silicon and a multilayer technology is therefore used to make metal field shields. The high voltage devices are N-channel DMOS which have better breakdown voltage characteristics than in the bipolar transistor counterparts and which, in addition, do not present the second breakdown phenomenon[1].

A video amplifier for one color channel is shown in Figure 1(*a*). In the IC there are basic elements: input differential amplifier with bipolar transistors (T_4, T_5), cascode amplifier with DMOS (T_1) and current driver with DMOS (T_2, T_3).

The gain of the video amplifier is externally adjusted by a series resistance in the input; (Figure 1(*b*)). The feedback resistance is connected between the input and the output. This gain adjustment is necessary to compensate for the gain difference between each color tube gun. The circuit contains a minimum number of components to obtain a low cost product.

The circuit output is connected to a 15pF capacitance (tube and wiring). This capacitance must be charged and discharged by a 100V supply in 150ns. The DMOS transistors T2 and T3 are designed to give 12mA with a 10V gate supply. To obtain the required risetime at the output, the T2 gate-drain capacitance must be charged at the same speed.

The gate-drain capacitance is 2.5pF, and therefore resistor R1 can be lower than 80kΩ. A 50kΩ value has been chosen. The dynamic range is calculated by the product of R1 and I1 of the current generator (4mA). The high-voltage DMOS transistor structure is shown in Figure 2. The vertical DMOS was chosen over the lateral DMOS because its structure permits one to reach a higher breakdown voltage[2]. This breakdown voltage is improved by limiting the electric field at the channel-drain junction periphery.

The technology is an adaptation of a classical IC bipolar technology to obtain high voltage capability[3]. Circuit components are junction isolated. High isolation breakdown voltage results from the choice of: the substrate resistivity (14–20Ω-cm), the depth of the diffused buried layer, the epitaxy characteristics (7Ωcm, 20μ).

To help isolate the 20μ thick epitaxial layer, P^+ foundations are implanted before epitaxial growth. DMOS fabrication requires the introduction of additional steps to classical bipolar fabrication to provide self-alignment of the P channel and the N^+ diffusion, channel implantation, and gate oxide layer.

The two aluminum interconnection layers are isolated by a composite nitride oxide layer. The first interconnection layer is used for the electric field shields and the DMOS gate. This metalization layer has sloped edges to help insure a good step coverage of the second aluminum layer.

The electrical characteristics of the integrated VDMOS appear in Figure 3. A 200V drain-source breakdown voltage has been achieved. The circuit shown in Figure 1 has been processed on a 3x2mm^2 chip. Figure 4 is a photomicrograph of the integrated circuit which contains three video amplifiers. The main specifications are given in Table 1. The total IC power dissipation in the worst case (white picture) is lower than 3W. For the other cases the total system dissipation is the same, but a part of the power is dissipated in the feedback resistances. With a 220V dc supply the output signal which can be obtained is shown in Figure 5.

The dc voltage (black level) is 120V. The dynamic range is 140V. The risetime is 150ns for 100V peak-to-peak.

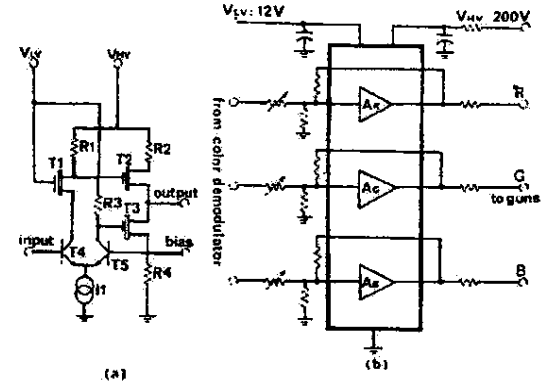

FIGURE 1—Circuitry contained in each amplifier (*a*); block diagram (*b*).

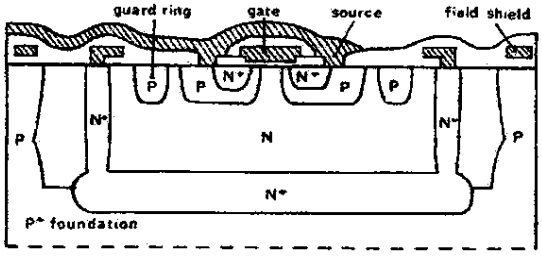

FIGURE 2—DMOS structure.

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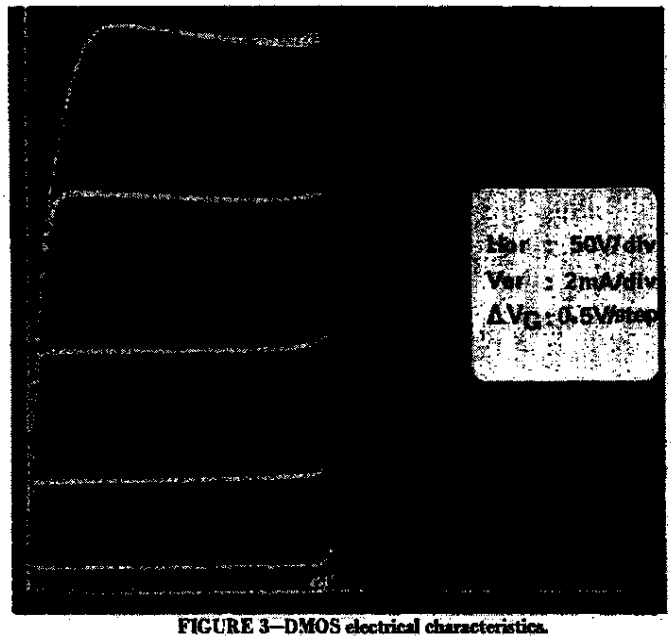
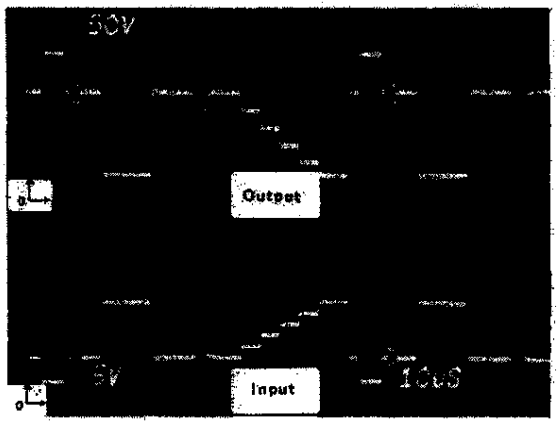


FIGURE 3—DMOS electrical characteristics.

maximum supply high voltage	300V
maximum supply low voltage	25V
maximum output current	100mA
dynamic range (V_{HV}:220V)	150V
bandwidth (3dB, 100Vpp)	5MHz
rise time (100Vpp)	150ns
fall time (100Vpp)	150ns
maximum IC power dissipation (V_{HV}:220V)	3W

TABLE 1—Electrical characteristics of the IC.



[Right]

FIGURE 5—Video signal characteristics: input (*a*); output (*b*).

FIGURE 4—Photomicrograph of the chip.

DX 624

LATERAL DMOS TRANSISTOR OPTIMIZED FOR HIGH VOLTAGE BIMOS APPLICATIONS

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ABSTRACT

Optimal placement of buried layer under a LDMOS transistor extends the usefulness of the device in high voltage BIMOS integrated circuits. Coupling the resurf effect and gate-underlaid concept results in a LDMOS transistor with uncompromised high voltage characteristics: Source-drain avalanche breakdown greater than 300 V and channel-substrate punchthrough breakdown greater than 200 V. The process utilized to fabricate the high voltage LDMOS transistor is a junction isolated epitaxial process. This enables high speed Emitter Function Logic and high voltage driver capability to be implemented on the same integrated circuit. Process modifications and device design necessary to realize the high voltage gate underlaid LDMOS transistor are described. A novel method for calculating the collector-emitter breakdown of NPN transistors is presented in order to compare process requirements of high voltage NPN and LDMOS transistors. A high voltage plasma driver with high speed logic capable of clocking at rates over 20MHz demonstrates the versatility of the process and the optimized LDMOS transistor.

INTRODUCTION

Integrated circuits which combine high voltage capabilities with high speed logic are becoming increasingly important as system designers seek to interface the ubiquitous microprocessor to a hostile (non TTL compatible) world.

Numerous approaches for combining high voltage devices and logic have been taken: all MOS[1], all bipolar[2], and combination bipolar-MOS[3] (BIMOS). Because of the variety of potential applications, it is not clear that one technology will meet all possible requirements. BIMOS technology is promising since it offers the capability of combining high voltage LDMOS transistors (LDMOST), very high speed bipolar logic, dense MOS logic, and medium to high voltage, high current bipolar transistors. In this work, an optimized LDMOST is utilized to meet the requirements for high voltage output drivers, and Emitter Function Logic (EFL) is used to attain the speed requirements of the logic circuitry. Through proper placement of the standard buried layer commonly used in junction isolated epitaxial processes, the source to substrate punchthrough voltage of the LDMOST was extended to 200 V without compromising any of the other parameters or increasing the process complexity.

DEVICE TECHNOLOGY

In deciding to choose BIMOS versus an all MOS or all bipolar process, it was felt that the versatility gained from combining optimal features of both technologies offset the increased process complexity. This first generation process combines metal-gate FETs with high performance bipolar transistors. The deciding factor in choosing BIMOS was the ease with which high-voltage LDMOST could be integrated into the standard bipolar process.

Calculations made using a simple one-dimensional BV_{CEO} model indicated that impractical epitaxial layer thicknesses were necessary to obtain the breakdown voltages required using an NPN transistor.

Following an approach by J. Dunkley, the equation for thickness-limited BV_{CEO} is:

$$BV_{CEO} = \frac{V_\infty}{\sqrt[4]{\beta+1}} \left[\frac{2 W_E}{W_\infty / \sqrt[8]{\beta+1}} - \left[\frac{W_E}{W_\infty / \sqrt[8]{\beta+1}} \right]^2 \right],$$

Where $W_\infty = 3.60 \times 10^{3} \sqrt{\frac{V_\infty}{N_D}}$

$V_\infty = 60 \left[\frac{N_D}{10^{16}} \right]^{-3/4}$,

N_D = doping density of epitaxial layer,
W_E = intrinsic thickness of the epitaxial layer,
β = common emitter current gain.

Using this equation and published LDMOST breakdown guidelines, it is possible to compare epitaxial thickness and resistivity requirements for NPN transistors and LDMOSTs.

Various breakdown phenomena are observed in LDMOST built with standard I.C. processes. These include oxide breakdown, PN junction avalanche breakdown, and P-P punch-through breakdown. In the design of a LDMOST careful attention must be paid to all these phenomena in order to insure the manufacturability and reliability of the device. Possible breakdown sites in an I.C. LDMOST are shown in Fig. 1.

The gate oxide integrity is insured by designing the device such that the lateral depletion spread encompasses the entire gate region well before the electric field at the edge of the depletion region would cause the gate oxide to break down. This effectively limits the electric field the gate oxide must withstand, which enables use of thin gate oxides (<1000 Å) without compromising device reliability.

Junction avalanche in the epitaxial region can occur at various sites: P-tub (surface), P-tub (bulk), P+ isolation, substrate, and even at the drain contact diffusion[6]. Flapping the P-tub diffusion with source or

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gate metallization, creating a stepped oxide profile, and making the P-tub reasonably deep (> 4.0 μm) extends the breakdown voltage of that junction. Choosing the drift region length and epitaxy thickness and doping correctly further extends the avalanche breakdown voltage by capitalizing on resurf action.[7] A thick thermal oxide and resurf maximizes the P+ isolation breakdown voltage. The goal is to make the substrate-epitaxy junction limit the avalanche breakdown voltage.

Punchthrough breakdown can occur at three sites: channel, P-tub to isolation laterally, and P-tub to isolation vertically. Channel punchthrough is easily optimized and has not been found to be a problem.[8] Lateral punchthrough is avoided by allowing the lateral spacing necessary to accomodate the desired voltage. Vertical punchthrough (VP_{S-SUB}) is not so easily optimized since changes in P-tub junction depth, and epitaxy thickness or doping level affect the avalanche breakdown voltage. Previously published work[9] reveals that for an optimized 300 V LDMOST, VP_{S-SUB}, occurs at approximately 80 V. This severly limits the versatility of the LDMOST as a high voltage circuit element. This limitation is eliminated by placing an N+ buried layer beneath the P-tub diffusion within its horizontal boundaries. This structure, which resembles the Gate Underlaid Transistor,[10] uncouples the requirements for high voltage avalanche breakdown from those of high source to substrate punchthrough voltage.

GATE UNDERLAID LDMOS TRANSISTOR

Difficulties inherent in integrating high voltage source follower LDMOSTs have been previously reported.[11] Solutions included thicker epitaxial layers or use of double acting resurf. Besides increasing process complexity, either option compromises some property of the device: density and possibly BV_{DSS} in the first case; R-on and current drive capability in the second case. The gate underlaid concept places no such constraint on the LDMOST.

The cross-section in Fig. 2 illustrates schematically the gate underlaid LDMOST. The same N+ buried layer used in the bipolar portion of the integrated circuit serves as the underlaid gate. Without the buried layer the device has characteristics identical to previously described LDMOST —high BV_{DSS} and low VP_{S-SUB} (Fig. 3A and 3B). If buried layer extends to beneath the N+ drain contact diffusion, BV_{DSS} is thickness limited and the device breaks down at approximately 100 V. By insetting the buried layer such that after out-diffusion it does not extend past the edge of the P-tub diffusion, BV_{DSS} is not degraded and VP_{S-SUB} is increased to over 200 V.

Since the undersized buried layer does not affect surface conduction, R-on and current drive capability are unaffected by its presence. The BV_{DSS} is not degraded because depletion regions extending from the P-tub and the substrate merge well before the LDMOST can be thickness breakdown limited. The undersized buried layer is electrostatically shielded from further increments in drain voltage.[10] Because of its high doping concentration, the buried layer increases the P-tub-to-substrate punch-through voltage. These results are summarized in Table I.

PROCESS TECHNOLOGY

A conventional junction isolated epitaxial processd was used to fabricate the BIMOS I.C. Basic process parameters are given in Table II. Of special importance with respect to breakdown voltage are the epitaxial doping density and thickness and the substrate doping density. These parameters were chosen so as to optimize the LDMOST. Two steps were added to the standard bipolar process flow (Table II) in order to integrate the conventional LDMOST — P-tub diffusion and a post-emitter gate oxidation. Both are critical since they determine the LDMOST's threshold voltage and stability. Recall that to realize the gate underlaid LDMOST no additional process steps are required since the standard buried layer is utilized for the underlaid gate.

CIRCUIT PERFORMANCE

To demonstrate the capabilities of the high voltage BIMOS process a 250 V display driver was fabricated. (Fig. 4) The requirement for high-voltage output drivers dictated the use of a 15 μm, 5Ω-cm epitaxial layer. This process does not lend itself to high-speed logic families, which are normally constructed on very thin, low-resistivity material. However, Emitter-Function Logic (EFL) is compatible with the required process, so it was used to implement the input latches and control circuitry that would have to operate at high data rates. Standard bipolar technology was used for the decoding function which provided the information to the output drivers.

When the circuit was evaluated, the input latches functioned very well, capturing data at speeds in excess of 20 MHz. The data was then decoded and displayed on the high-voltage LDMOS outputs. The EFL provides a good compromise between the high-speed, high-current ECL family, and the other lower speed, lower power logic families such as metal-gate CMOS, possible on the process. The total power dissipation of the device was only 75 mW, notwithstanding its high-speed capabilities. Further evaluation showed all AC and DC characteristics of the logic portion of the chip were well within acceptable limits.

CONCLUSION

An optimized LDMOS transistor easily integrated into a standard bipolar process has been demonstrated. The resurf effect is coupled to the gate underlaid concept resulting in a LDMOS transistor with BV_{DSS} > 300 V and VP_{S-SUB} > 200 V. This extends the usefulness of the LDMOS transistor as a circuit element without increasing process complexity. The BIMOS process discussed was used to fabricate a high-voltage display driver circuit using the LDMOS transistors as the output drivers and EFL to implement the input latches and control circuitry.

ACKNOWLEDGEMENTS

We would like to thank K. Drozdowicz and J. Saltich for their support, Motorola Fabrication Group for device processing, and Phyllis Evangelo for manuscript preparation.

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DEVICE	BV_{CEO}	BV_{CBO}	VPT_{BS}	BV_{DSS}
NPN/DMOS WITH BURIED LAYER	52	136	200	100
NPN/DMOS WITH NO BURIED LAYER	250	320	160	330
NPN/DMOS NPN WITH MODIFIED BURIED LAYER *	UNDER STUDY	310	200	330

*5μM UNDERSIZE OF BASE (OR P-TUB) DIFFUSION

TABLE I
EFFECT OF BURIED LAYER - DMOS/BIPOLAR

Substrate	10 Ω-cm	(111)
Buried Layer	20 Ω/□	8 μm
Epitaxy	5 Ω-cm	15 μm
Isolation	5 Ω/□	18 μm
Deep Collector	4 Ω/□	14 μm
P-Tub *	300 Ω/□	5.0 μm
Base	125 Ω/□	3.0 μm
Emitter	5 Ω/□	2.0 μm
Gate Oxide *	-	100 nm
Pre-Ohmic	-	-
Metallization	-	150 nm
Final Passivation	-	500 nm

* Added Steps

TABLE II
PROCESS PARAMETERS

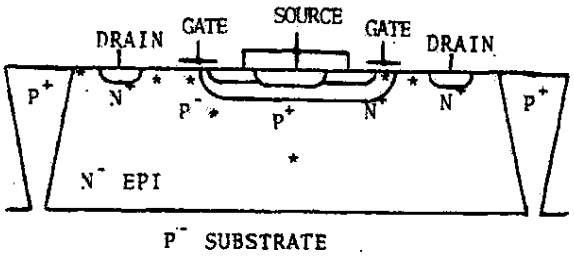

FIG. 1
POTENTIAL BREAKDOWN SITES IN A LDMOS TRANSISTOR

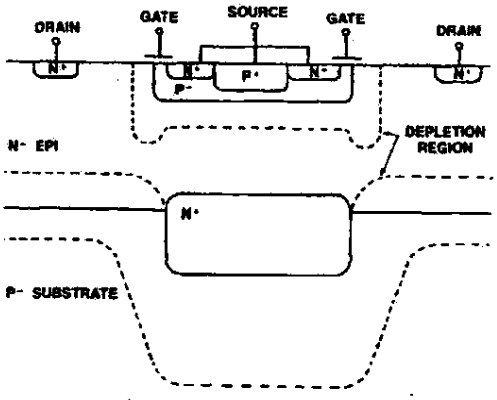

FIG. 2
GATE UNDERLAID LDMOS TRANSISTOR

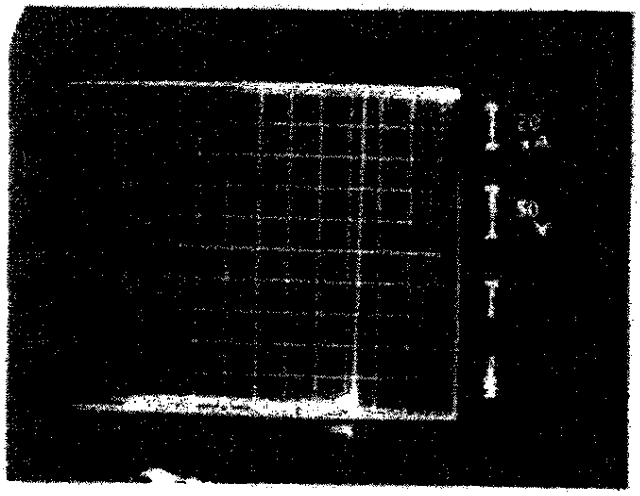

FIG. 3A
LDMOST BV_{DSS} CHARACTERISTICS

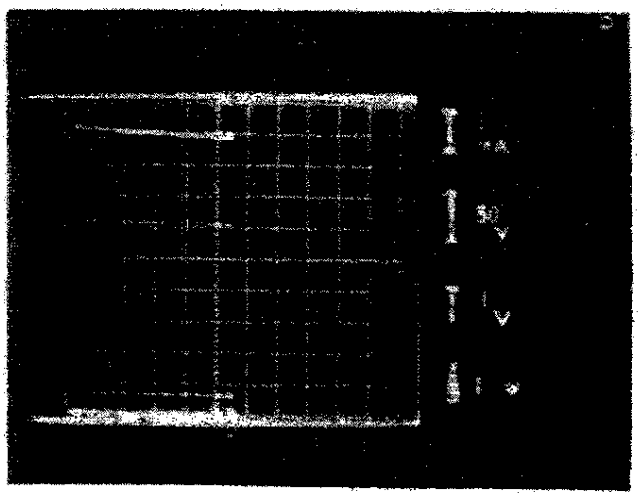

FIG. 3B
LDMOST I_D-V_{DS} CHARACTERISTICS

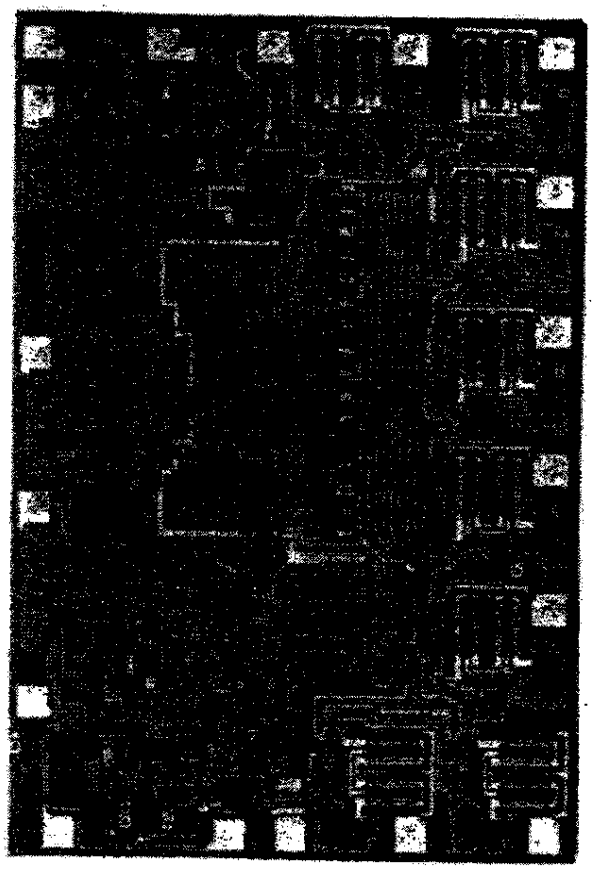

FIG. 4
BIPOLAR - DMOS
PLASMA DISPLAY DRIVE

DX 625

SESSION XVII: TELECOMMUNICATION CIRCUITS

FAM 17.2: 400V Switches for Subscriber Line Interface

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Bell Telephone Manufacturing Co.

Antwerp, Belgium

SEVERAL SWITCHING functions in current subscriber line interfaces of digital telephone exchanges are performed by electromechanical relays. Replacement by solid state switches has been proposed for reduced cost and size and improved reliability. The main specifications are: up to 400V blocking voltage, 100mA dc current and 10Ω ON-resistance. Recent developments in this field are based on junction isolation and additional high voltage power supplies[1], or on optical coupling and special packaging techniques[2]. This paper will discuss a switch based on complete dielectric isolation between the low voltage control inputs and the high voltage output terminals, while offering full integration of switches, control and decoding logic.

The schematic of Figure 1 introduces the main building blocks of the monolithic switch. The low voltage decoder is separated from the high voltage circuits by the pair of coupling capacitors C_c. These integrated capacitors serve a double purpose:

(1)—They provide the dielectric isolation between input and HV output, allowing the output terminals to float from –400V to +400V with respect to the input logic ground, without affecting the functioning of the switch.

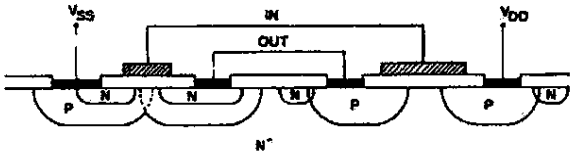
(2)—The capacitors C_c couple the control signals ϕ_1 and ϕ_2 to the HV control circuit. The value of these coupling capacitors is limited to about 15pF to keep a relatively high degree of integration. Consequently, the driving power for the HV devices can only be obtained by control signals at high frequencies. Experimental evidence indicates that a clock rate of 100kHz is sufficient.

The control circuit fulfills three basic functions.

(1)—A diode bridge converts the control signals from the coupling capacitors into a dc driving voltage for the switch.

(2)—Detection of the ON/OFF information contained in the control signals and generation of the appropriate gate driving voltage. This function is implemented using two PMOS transistors in an exclusive OR arrangement; Figure 1. Two anti-phase signals generate a high output voltage over the resistance to drive the switch in the ON (closed) position. If ϕ_1 and ϕ_2 are in phase or both zero, the output of the exclusive OR becomes zero, and the switch is open.

(3)—The control circuit must provide sufficient noise margin against spurious signals appearing at the output terminals.



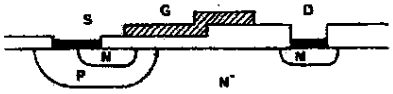


FIGURE 3—Cross sections of a DDMOS and PMOS transistor forming a DCMOS inverter gate, and the HV DMOS.

[Right]

FIGURE 1—Schematic of the monolithic switch.

Slow transients will not affect the functioning of the switch, since the latter is allowed to float with respect to the logic ground. Fast transients can appear as a common mode signal at the input terminals of the exclusive OR gate and will then open the switch. In this way the switch and interconnected circuits are protected against fast transients at the high voltage terminals.

Vertical DMOS transistors are the basic devices for the high voltage switches. They provide a good compromise between ON resistance and breakdown voltage[3], without causing latching problems; Figure 2. To reduce the drain resistance and thus the ON resistance, a buried layer is introduced during the fabrication of the dielectrically isolated (DI) wafers. Two high voltage DMOS transistors, in separate DI tubs, are connected back-to-back with common source and gate; Figure 1. The resulting bidirectional switch can withstand up to +400V or –400V in the OFF condition and conduct from +100mA to –100mA dc in the ON condition. Surge current capability depends on the amplitude of the control signals ϕ_1 and ϕ_2 and can be larger than 1A.

The input decoding logic converts the input signals into the appropriate control signals ϕ_1 and ϕ_2 for each of the integrated switches. To obtain full input flexibility and a high degree of integration, a HV DMOS compatible CMOS technology (DCMOS) is used. A substrate MOS transistor yields the PMOS, while a double DMOS (DDMOS) device is used as NMOS transistor; Figure 3. The DDMOS consists of two single DMOS devices shifted close together, such that the P channel regions overlap under the gate area. Thus, taking advantage of the double diffused characteristics of the DMOS structure, a self-isolating DDMOS device results. This technique eliminates the additional P isolation well of conventional CMOS processes. Non-critical layout tolerances are maintained in the DDMOS transistor. The gate length is determined by the NP clearance of the HV DMOS design and is large enough to accommodate process variations. The DDMOS devices have a mask gate length of 7μm and an effective gate length of 3.5μm.

The threshold voltages of the DCMOS devices are fixed at +1.3V for the DDMOS transistor and –1.3V for the PMOS. The resulting DCMOS process is fully compatible with the high voltage DMOS technology. The supply voltage can range from 3V to 16V, allowing easy interfacing with the outside controlling logic. Any type of input format, also an address bus, can be used to control the switches. A decoding logic to generate the necessary driving signals is easily implemented.

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The author wishes to thank R. Cohen and J. Pernyeszi of ITT Shelton and R. Hochreutiner of STR Zurich for their generous advice.

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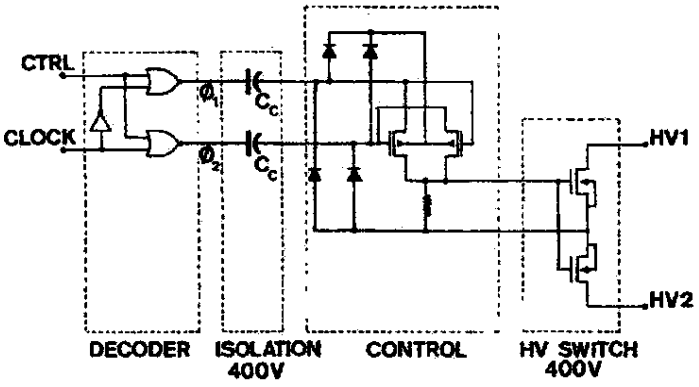
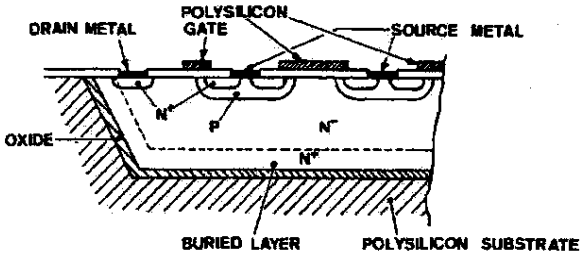




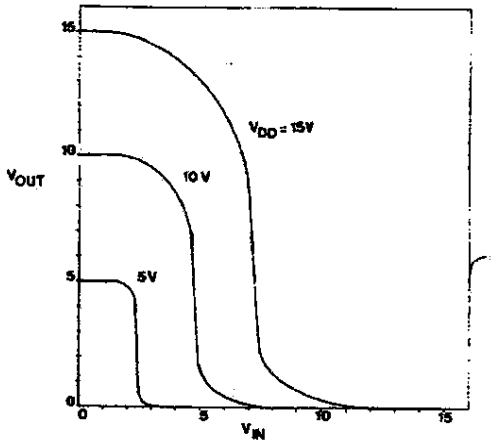


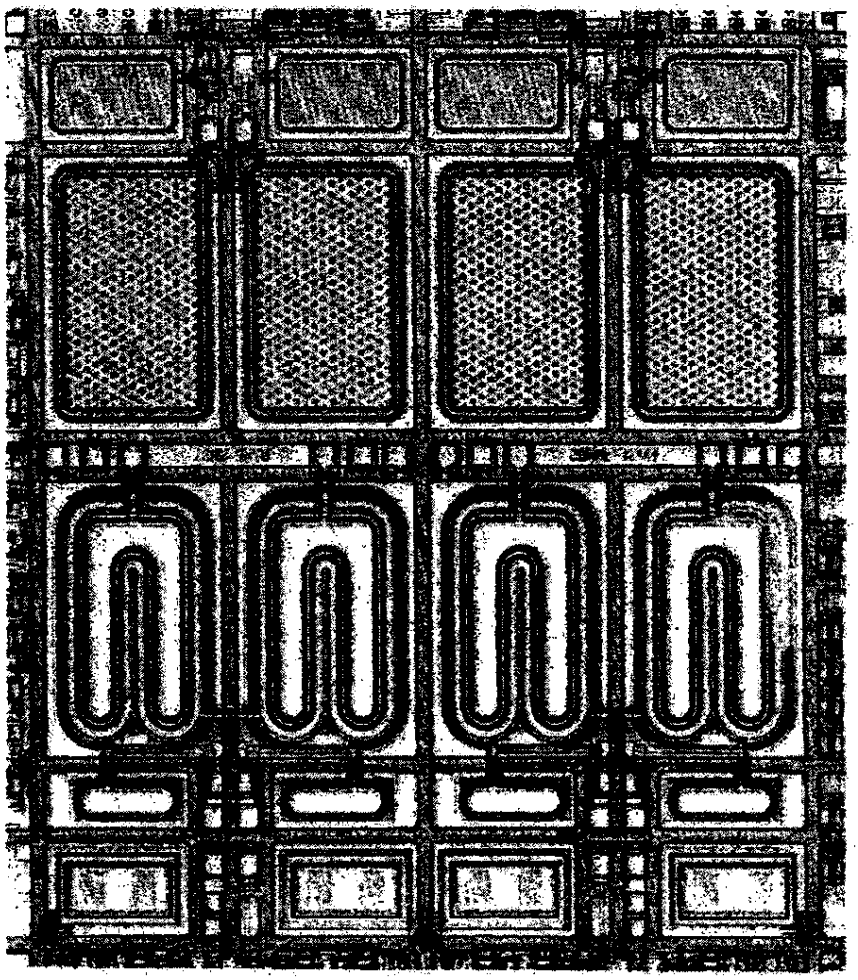
FIGURE 4—Transfer characteristics of a DCMOS inverter gate for supply voltages VDD = 5V, 10V, 15V.

[Left]

FIGURE 2—Cross section of the DMOS transistor in a dielectrically-isolated bucket.

[Below]

FIGURE 5—Chip photo. Active area 5.0x5.6mm^2.



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Effects of Drift Region Parameters on the Static Properties of Power LDMOST

SEL COLAK

Abstract—The effects of the drift region geometry and the physical parameters on the thin layer (resurfed) lateral DMOS transistor operation have been studied for both the static on-state and the off-state. The variations of breakdown voltage with drift region parameters were investigated using numerical modeling and compared to the experimental results. The operation of the LDMOST in the on-channel condition was modeled semi-emphirically. The analytical and experimental results show that the operation of the device depends strongly on the geometry and the physical parameters of the drift region, particularly at high gate voltages and low drain voltages. Design guidelines for the lateral DMOS transistor for switching applications are discussed.

Introduction

It has recently been noted that the breakdown voltage of the lateral double-diffused MOS (LDMOS) transistor can be optimized by adjusting the drift region epitaxial thickness and resistivity [1]. This optimization results from *re*duced *sur*face *f*ields (resurf) and has been observed previously for JFET's and BJT's [2]. However, the small drift region thickness required to obtain the optimum breakdown voltage results in an increase in the minimum on-resistance of resurf devices. In order to be able to design well-optimized power LDMOS devices, the effects of drift region parameters on the breakdown voltage and on the on-resistance have to be understood. The present article describes the models developed for the on-resistance and the breakdown voltage of the LDMOST.

The on-resistance model of the LDMOST is developed analytically taking into account the current spreading effects in the drift region. This model is extended semi-empirically to current and voltage levels high enough to cause saturation within the drift region. The results from this model explain the drift region limited on-resistance and saturation in the LDMOST at high gate voltages [3] and compare well with experimental observations.

The avalanche breakdown modeling is done numerically in two dimensions using the computational method previously reported [4]. With this breakdown model the effects of various drift region parameters on LDMOST avalanche breakdown are studied. The results from breakdown modeling fit the experimentally obtained results and explain the observed improvements in breakdown voltage.

The first section of this article studies the behavior of the on-resistance. First, the on-resistance of the LDMOST is found at low drain voltage and currents, assuming the channel region contributions to the on-resistance is negligible. Then the effects of saturation related to the drift region and the channel region are taken into account to model the on-resistance of the device at high bias conditions. Following the on-resistance model, the results of the two-dimensional analysis for breakdown is presented. This latter section includes a design example for a 400-V device which makes use of these models to obtain significantly reduced on-resistance for a given silicon area.

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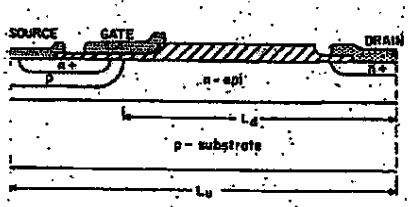

Fig. 1. Channel and drift region of the LDMOST. L_d is the length of the drift region. L_u is the unit cell length.

On-Resistance

The limiting drift region on-resistance of the LDMOST was previously computed by Pocha and Dutton [5]. This analysis assumed infinite epitaxial layer thickness and used two empirical constants. Thus it is not applicable for thin layer structures. It is possible, however, to compute the drift region limiting on-resistance for finite epitaxial drift region thicknesses without the need of using any empirical parameters. The on-resistance of the LDMOST can be separated into two parts, due to the channel and the drift region. In the present study, the drift region is defined as the n-type epitaxial region of length L_d between the channel end and the center of the drain contact (Fig. 1). The on-resistance figure-of-merit for a device with active area A ($A = L_u Z$, where L_u is the unit cell length and Z is the channel width) is defined as $R_{on}A$ where R_{on} is the net on-resistance. This figure-of-merit is to be minimized for a given breakdown voltage to get devices with optimum design parameters.

With increasing gate voltage, the on-resistance of the channel region decreases while that of the drift region stays nearly constant. At high enough gate voltages, the channel can contribute negligibly to the total on-resistance, which results in a saturation value depending only on the parameters of the drift region. At the high gate voltage necessary to turn the channel on strongly, there is a heavy accumulation layer beneath the extention of the gate metal over the drift region. At low drain voltages, this accumulation layer acts like an equal potential source of electrons. The conduction between this accumulation layer and the heavily doped n^+ drain contact region is then ohmic. Since the current spreading can be significant in some

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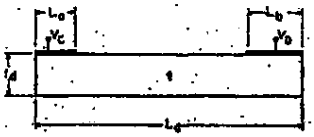


Fig. 2. Model for the drift region resistance assuming heavy accumulation layer beneath the gate metal. V_C and V_D are potentials at the end of the channel and at the drain, respectively. L_a, L_b, and L_d are the accumulation layer length, drain collection region length, and the drift region length, respectively. t_d is the drift region thickness, and ρ is the resistivity of the drift region epitaxial material.

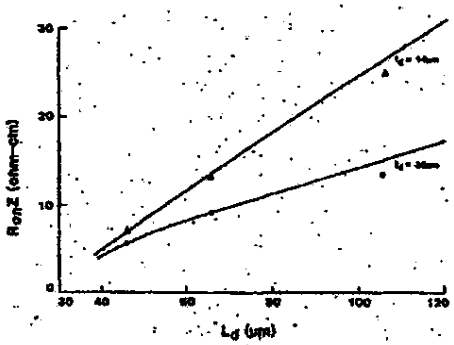


Fig. 3. Comparison of minimum drift region resistance values as a function of drift region length obtained from (1) (solid lines), and experimental values (discrete figures) for two different layer thicknesses, t_d = 14 μm, and 30 μm. The remaining parameters of the drift region are: L_a = 14 μm, L_b = 22 μm, and ρ = 4.5 Ω · cm. Note that the resistance values are normalized with respect to the width of the device z.

cases, the resistance of such a region is found following a conformal transformation. The conformal transformation maps the irregular geometry of the drift region shown in Fig. 2, to a simpler geometry where the resistance value is found easily. The details of this transformation are given in Appendix I.

The form of the resultant on-resistance expression for the drift region (for drain voltages below saturation) is

$$R = \frac{\rho}{Z} f(L_d, t_d, L_a, L_b). \tag{1}$$

The function $f(L_d, t_d, L_a, L_b)$ depends only on the geometrical parameters of the drift region and its expression is given in Appendix I. ρ and Z are the resistivity and the width of the drift region. The calculated values of the drift region resistance obtained from (1) are compared with experimental values of Fig. 3.

The experimental LDMOS devices were fabricated using an n-type epitaxial layer with approximately 1×10^{15} cm^{-3} doping (4.5 Ω · cm) on a p-type substrate with 1.5×10^{15} cm^{-3} doping. The resistance values given in Fig. 3 are normalized with respect to the width of the device together with the net resistance values. The total channel widths for all these devices were 1 mm.

The experimental values of the drift region resistances were obtained by applying gate potentials high enough to saturate the total on-resistance at its minimum value. The drain potential was kept at about 2 V during the measurements. This keeps the device in the linear operation mode. As seen from

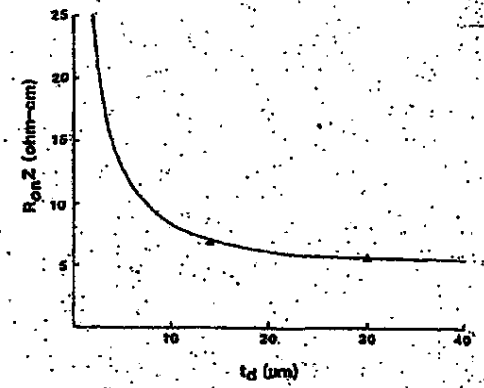


Fig. 4. The effect of epitaxial thickness on the normalized drift region on-resistance for the device with L_d = 46 μm. The remaining parameters of the device are the same as the ones in Fig. 3.

Fig. 3 the calculated resistance values from (1) fits the experimental results very well without the need of any empirical factors.

In order to be able to see the effect of epitaxial layer thickness, (1) is used to compute the limiting drift region on-resistance for different epitaxial layer thicknesses for an LDMOST with L_d = 46 μm. The results are plotted in Fig. 4, together with the available experimental points. Note that, as expected, for thicker epitaxial layers the minimum drift region resistance saturates and becomes nearly independent of epitaxial layer thickness. For thin drift regions ($t_d/L_d \ll 1$) the limiting drift region on-resistance varies with a dependence of the form $R_{on}Z = a/t_d$. Additional calculations show that the constant a has a functional dependence on L_d which reduces to $a = \rho L_d$ for $(L_a + L_b) \ll L_d$. For very thick drift regions, the dependence of $R_{on}Z$ on t_d disappears and $R_{on}Z$ is constant. Between these limits, $R_{on}Z$ has a more complex dependence on t_d.

The length L_a of the gate metal extension over the drift region also affects the limiting drift region on-resistance. The normalized on-resistance values as a function of accumulation layer length beneath this gate metal extension were calculated for a constant drift region length and for four different epitaxial thicknesses and plotted in Fig. 5. As expected, the on-resistance increases as L_a gets shorter, and this dependence becomes stronger for decreasing epitaxial layer thicknesses.

As the voltage at the drain is increased to high values, the device starts responding nonlinearly and the current saturates. For small gate voltages, this saturation will occur in the channel. For high gate voltages where the channel is turned on strongly, which is the case for power switching devices, the saturation occurs in the drift region. The channel and the drift region models including saturation effects are developed in the following paragraphs.

Understanding the behavior of the LDMOST channel region requires a detailed 2-D analysis taking into account short-channel, nonuniform doping, and diffusion current effects. These problems have been investigated, mostly using semi-empirical analytical models. For example, the effects of diffusion currents on MOS transistor operation were studied by

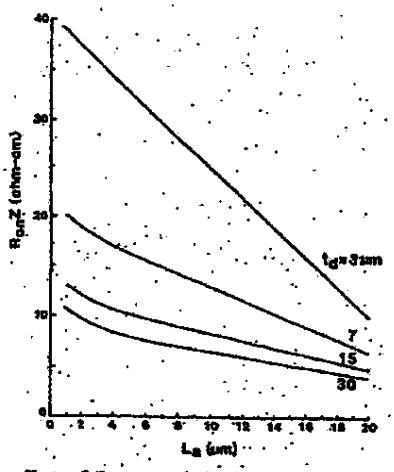


Fig. 5. The effects of the accumulation layer length L_a on the limiting on-resistance of the LDMOST for different epitaxial layer thicknesses. Drift region length is L_d = 46 μm. Other parameters are the same as given in Fig. 3.

and Sah [6], Masuhara and Muller [7], Harper and Thomas [8], and Kennedy and Murley [9]. The short channel effects and velocity saturation were studied by, for example, Armstrong and Magawan [10], Baum and Beneking [11], Rodgers *et al.* [12], Compeers *et al.* [13], and Klaassen and Groot [14]. The effects of diffusion profile on the DMOS channel were studied by Lin and Jones [15] and D'Avanzo *et al.* [16].

The channel region models developed in these studies usually contain empirical parameters which are varied to fit experimental results. For the purposes of the present study, the inaccuracies caused by these empirical MOS channel models will not be significant. This is due to the fact that the drift region resistance dominates the overall device characteristics at high gate voltages, even near channel saturation. The channel region behavior included in the present study will therefore be a semi-empirical channel region model similar to the one given in [5].

If the potential at the drain end of the channel is taken to be V_c and the gate potential is V_G, then the channel current per unit drain width is given by

$$\frac{I_{ch}}{Z} = \frac{\mu}{\ell} g(V_c, V_G) \tag{2}$$

where μ and ℓ are the effective mobility and the effective length of the channel, respectively. All three terms on the right influence the channel saturation. The $g(V_c, V_G)$ term is taken into account using a critical field value, which is defined as the electric field at which the electrons will reach their saturation velocity. The functional dependence of the term $g(V_c, V_G)$ on these conditions and on the physical properties is summarized in Appendix II.

However, even before the critical field is reached, there is a reduction in mobility of the carriers in the channel. This variation has been modeled by dividing the mobility into regions with different dependences on the field [17]. The same behavior can also be described by the empirical expression

$$\mu = \frac{\mu_G}{\sqrt{1 + \left(\frac{V_c/\ell_0}{E_M}\right)^2}} \tag{3a}$$

where ℓ_0 is the channel length at zero bias, and E_M is an empirical electrical field value which is taken to be 1×10^4 V/cm. This expression is valid up to a channel voltage $V_{cm} = \ell_0 E_M$, which is defined as the voltage at which the channel region starts saturating due to velocity saturation. At higher voltages than V_{cm}, the carrier mobility stays constant in the unsaturated regions, while the carrier velocity is constant in the saturated regions. This is due to the fact that the saturated regions continue supporting the additional electric fields with increasing V_c while the remaining unsaturated regions of the channel maintains a nearly constant average electric field values. The areas which reach the velocity saturation require some channel length modulation as will be described shortly. μ_G in (3a) is the effective mobility in the channel after the effect of gate potential is taken into account and is given by [5]

$$\mu_G = \mu_0 \left(\frac{7 \times 10^4 t_{ox}}{V_{GT} - V_c/2}\right)^{0.3} \tag{3b}$$

where again μ_G stays constant above $V_{cm} = \ell_0 E_M$, for the same reason given above. μ_0 in (3b) is the unsaturated effective electron surface mobility and its value is 650 cm^2/(V · s) [5]. V_{GT} is the effective gate voltage defined in Appendix II.

In this analysis, the effects of saturation on reducing channel length will be included empirically by channel length modulation parameters. The weak inversion regions which are at the higher potential and the higher doped regions as are seen from the dependence of the threshold voltage on the channel doping [15], have the highest electric fields. It is assumed that the saturation, due to either mobility reduction or pinchoff, starts at a highly doped region of the channel and spreads in both directions, decreasing the channel length. This is due to the higher potentials at the drain end and higher doping levels towards the source end. This modulation slows down as the channel starts constituting only the lowly doped areas between the source and the peak channel doping. This behavior can be modeled by the empirical relation

$$\ell = \ell_0 \left[1 - \frac{\alpha(V_c - V_{csat})}{1 + \beta(V_c - V_{csat})}\right] \tag{4}$$

where α and β are empirical parameters. The saturation voltage V_{csat} is defined by (23) in Appendix II. The expression given by (4) eliminates the sharp corners in the modeled I–V characteristics due to the shortening of the channel at low gate voltages. This was taken into account by Scharf and Plummer [18] for DMOS devices by using the analysis of Frohman-Benchkowsky and Grove [19].

The channel region model is thus given by the set of relations in (2), (3), and (4). Although there are rather crude approximations in this model, the resultant errors caused will be negligible in the range of operation which is of interest for power

switching LDMOST due to the dominating effects of the drift region.

The model for the drift region takes into account three different effects, viz., modulation of the effective accumulation length beneath the gate, velocity saturation of carriers in the drift region, and decrease in effective epi thickness due to depletion along the epitaxial junction. The conductivity and effective length of the accumulation layer in the epi beneath the gate are dependent on the voltage and current levels. This layer has a position dependent current due to the carrier losses to the epitaxy beneath it. As a first-order approximation, it is assumed that the fields perpendicular to the accumulation layer vary linearly from the channel to the end of the layer, where the field reaches a maximum value given by E_{max}. Then, the position dependent current I_a along the accumulation layer is given by

$$\frac{I_a(x)}{Z} = \frac{I_D}{Z} - \int_0^x J_1(x')\,dx' \tag{5}$$

where $J_1(x)$ is the current density at the position x lost by the accumulation layer towards the bulk epitaxial layer and I_D is the drain current. I_a goes to zero at the end of accumulation layer at $x = L$. $J_1(x)$ is given by

$$J_1(x) \simeq \frac{E_{max}}{\rho L} x = \frac{2}{L^2}\frac{I_D}{Z} x \tag{6}$$

where ρ is the epitaxial layer resistivity.

Expressions (5) and (6), together with a simple analysis of MOS-type conduction, yield the following for the drain current for voltage $V_A \leqslant V_G$:

$$\frac{I_D}{Z} = \frac{\mu_n C_{ox}}{2L/3}\left[\left(V_G - \frac{V_A}{2}\right)V_A - \left(V_G - \frac{V_c}{2}\right)V_c\right]. \tag{7}$$

V_c and V_A are the potentials at the end of channel and at the end of the accumulation layers, respectively, C_{ox} is the unit area gate oxide capacitance, and μ_n is the electron mobility in the accumulation layer. Up to a certain level of drain current, the accumulation layer length will not change. However, after V_A reaches the saturation voltage, which is close to the gate potential value, the length of this accumulation layer starts decreasing. The value of the drain current at which saturation starts due to the accumulation layer is found from (7) by the condition $V_A \simeq V_G$. This current is given by

$$\left(\frac{I_D}{Z}\right)_{sat} = \frac{\mu_n C_{ox}}{AL_a/3}\left[V_G^2 - (2V_G - V_c)V_c\right] \tag{8}$$

where L_a is the length of the accumulation layer for drain voltages up to the saturation voltage of the accumulation region as shown in Fig. 2.

Further, increases of the drain current result in a decrease in the accumulation layer length while the potential of the drift region end of the shortened layer stays at about $V_A = V_G$. Equation (7) can then be used to determine the new length L_{ac} and, when combined with (8), yields

$$L_{ac} = L_a \frac{(I_D/Z)_{sat}}{(I_D/Z)}$$

which is valid for $(I_D/Z) > (I_D/A)_{sat}$. From this, an empirical effective accumulation layer length L_e is defined which combines the high and low current lengths of the accumulation layer and provides a smooth transition layer between them.

$$L_e \simeq L_a \frac{(I_D/Z)_{sat}}{(I_D/Z)_{sat} + (I_D/Z)}. \tag{9}$$

This effective accumulation length is assumed to have high enough conductivity to be considered a metallic contact in the conformal mapping analysis. This condition is satisfied at high gate voltages at which the effective conductivity of the accumulation layer becomes much larger than the conductivity of the epitaxial layer.

The mobility reduction effects within the accumulation layer are included in the analysis by similar expressions as given in (3a) and (3b). However, the zero field surface mobility for the accumulation layer was taken to be 800 $cm^2/V \cdot s$ to take into account the reduced effect of impurity scattering.

The velocity saturation effect within the bulk of the epitaxial drift region is modeled by assuming a mobility reduction similar to that in the accumulation layer by using the same functional relationship as in (3a). For analytical convenience, this mobility reduction is expressed in terms of an equivalent effective resistivity given by

$$\rho_e = \rho\sqrt{1 + \left(\frac{E_{long}}{E_m}\right)^2} \tag{10a}$$

where

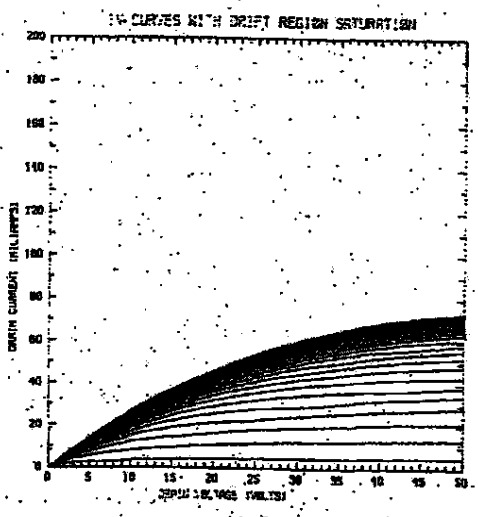
$$E_{long} = (V_D - V_c)/(L_d - L_c). \tag{10b}$$

With the effective accumulation layer length given by (9) and the effective resistivity given by (10), the drift region resistance can be calculated from (1) using the relations in Appendix I. It is necessary to include the effective thickness of the drift region which is a function of the drain potential. This is due to the effect of the substrate-epitaxial junction depletion region. Although this depletion region has two-dimensional effects, it was found that a simple one-dimensional geometry gives satisfactory results compared to experiments. The effective drift region thickness for one dimension is

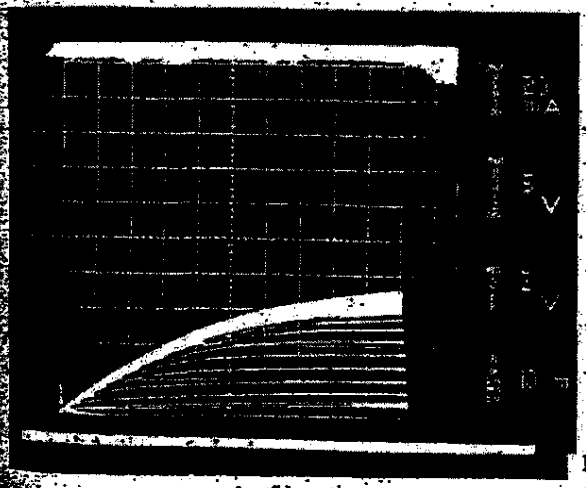
$$t_{de} = t_d - \sqrt{\frac{2\varepsilon_s N_A V_D}{qN_D(N_A + N_D)}} \tag{11}$$

The last term on the right-hand side of (11) is the depletion region width in the n-drift region when V_D is applied across the p-n junction. N_A and N_D are the substrate and epitaxial layer doping densities, respectively. Although the reverse bias across this junction is much lower in the channel region, this does not affect the results very much. This has two causes. First, the channel-to-epitaxy junction also has a depletion region and thus decreases the effective drift region thickness near the channel. Second, the currents near the channel flow closer to the surface which minimizes the errors in effective drift region thickness.

Even at high drain voltage, if the gate potential is also high, the effect of the drift region resistance still dominates the



(a)



(b)

Fig. 6. (a) Calculated I–V characteristics of the LDMOST with the saturation effects taken into account. If the saturation effects were neglected the envelope of the I–V characteristics would be a straight line with a slope equal to the minimum on-resistance at small drain potentials. (b) Experimental I–V characteristics of the same device. Drift region parameters in both cases are $L_d = 66$ μm, $t_d = 14$ μm, $L_a = 14$ μm, $L_b = 22$ μm, and $\rho \simeq 4.5$ Ω · cm.

characteristics of the device due to the saturation effects described above. An example of this behavior is shown in Fig. 6(a) for the calculated characteristics. This compares with the experimental characteristics shown in Fig. 6(b). The empirical channel modulation parameters (4) for the device modeled, are chosen to be $\alpha = 0.5$ and $\beta = 1.3$. The unmodulated channel length is $\simeq 2.5$ μm, $L_d = 66$ μm, and $t_d = 14$ μm. The remaining parameters which are defined in Fig. 2 are $L_a = 14$ μm, $L_b = 22$ μm, and $\rho = 4.5$ Ω · cm.

Using these models the saturation effects of the drift region are studied at high drain and gate voltages. Fig. 7 gives the

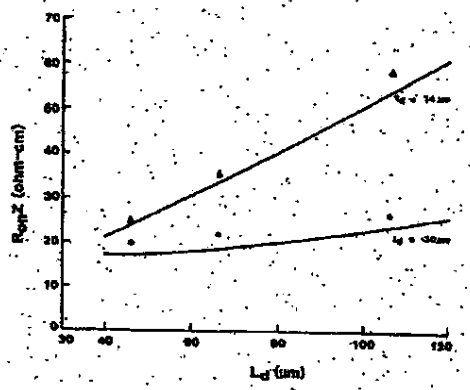


Fig. 7. The limiting on-resistance of the LDMOS transistor, at $V_D = 50$ V drain potential, as a function of the drift region length for two different epitaxial thicknesses. The remaining parameters of the drift region are the same as given in Fig. 3. The corresponding experimental values are shown with discrete figures.

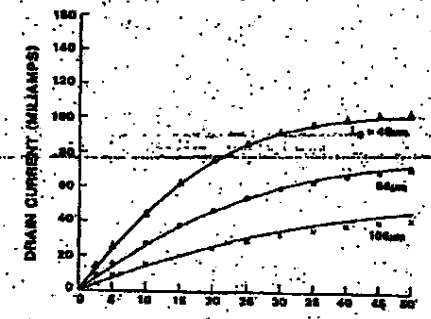


Fig. 8. Drift region saturation effects in devices with $t_d = 14$ μm, and for three different drift region lengths, $L_d = 46$, 66, and 106 μm. Other parameters are the same as given in Fig. 3. The solid lines are the calculated curves, and discrete figures are experimental measurements at high gate voltages.

limiting on-resistance of the LDMOS devices as a function of drift region length at a drain voltage of $V_d = 50$ V. The epi thicknesses are given in the figure and the remaining drift region parameters are as above. The experimental measurements were determined with high enough gate voltage applied to insure the channel region resistance being negligible compared to the drift region resistance. The limiting drift region resistances are significantly greater at this drain voltage than at low drain voltages (Fig. 3). Fig. 8 shows how the device current at high gate bias saturates as the drain potential is increased for three different drift region lengths and for $t_d = 14$ μm. Note that the drain current saturates more readily as the drift region length becomes shorter.

It is clear from these results that the effects of drift region resistance on the characteristics of power DMOS transistors are substantial. The channel region resistance of these devices usually becomes very small compared to the drift region resistance when the device is in its on-channel state. The device is limited by its unsaturated drift region resistances at low drain voltages and this resistance remains the major portion of the

total on-resistance even at high drain voltages due to its saturation properties. The transconductance of the device is also affected by this saturation and it approaches zero as the saturated value of the drift region resistance is reached. These points are important for switching and large signal power lateral DMOS transistors.

Breakdown Voltage

Breakdown in an LDMOST may occur due to either punchthrough within the channel or avalanching at one or more of the p-n junctions in contact with the n-drift region. The punchthrough breakdown in the channel has been studied by Pocha *et al.* [20]. Their results show this type of breakdown can easily be improved at the expense of the threshold voltage. As it will be explained shortly, this tradeoff between the threshold voltage and the punchthrough breakdown in thin layer resurfed LDMOST is less severe due to the nearly homogeneous field distribution in the drift region. Thus the punchthrough breakdown of thin layer LDMOST can easily be improved by changing the properties of the double diffused channel region without excessively compromising the remaining device characteristics.

Improving the avalanche breakdown at the p-n junctions in contact with the epitaxial drift region, however, requires a good understanding and careful design of drift region parameters in order not to degrade other properties of the device. This is due to the fact that these parameters affect the on-state device characteristics drastically, as explained in the previous section. The optimization of avalanche breakdown in the LDMOST requires the determination of the potential distribution within the device. Although for thick layer devices, an approximate empirical model [21], [22] can be used, for thin layer devices this approach introduces very large errors and is not usable. The accurate potential distribution can be found by a numerical solution [4] of the nonlinear Poisson's equation using a two-dimensional depletion region method [23].

The geometry of the lateral DMOS transistor, simplified for modeling purposes, is shown in Fig. 9. Fig. 10 shows the off-state constant potential contours within this device at 250-V drain reverse voltage. The source region in Fig. 10 is omitted because it has no significance in the off-channel condition in the absence of punchthrough. The contour lines crowd near the curved portion of the channel junction and under the edge of the gate metal. These indicate high electric field regions which may lead to avalanche breakdown.

The possible avalanching paths passing through the peak electric field points were found by following the electric field direction from these points. The multiplication factors along these paths were calculated by using the ionization rates given by Overstraeten and DeMan [24]. These multiplication factors were $M_p \simeq 1.5$ and $M_n \gg 1$ near the curved portion of the channel doping and close to the edge of the gate metal. These numbers indicate that these regions are very close to the electron initiated avalanche breakdown. It should be noted that unless M_p (hole multiplication factor) also increases further, the high value of M_n (electron multiplication factor) will not have any significance. The avalanche multiplication process is an electron-hole pair generation mechanism. Unless holes are extracted from the depletion region, they will act as additional recombination centers in a space charge area and will prevent the avalanche breakdown. For avalanching, M_p must also become high to provide the high hole current at the p end of the depletion region equal to the electron current on the other

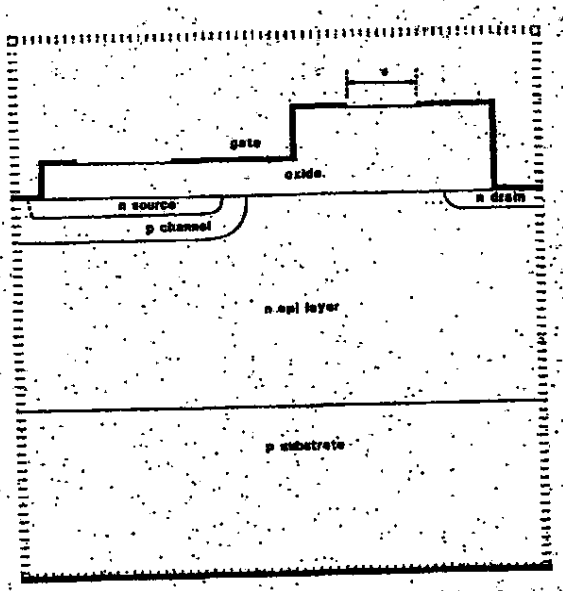


Fig. 9. Geometry of the active region of a DMOS transistor for two-dimensional modeling the breakdown voltage. Note that the source and channel are shorted to each other by the source metal. The device is drawn to scale with 1 μm/div everywhere except the vertical scale has a 0.1 μm/div scale range between the two extreme sides of the oxide layer.

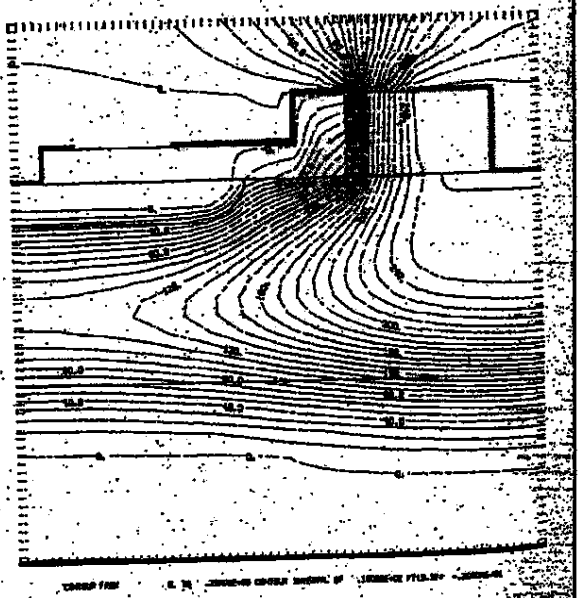


Fig. 10. Potential contours for the DMOS of Fig. 9 at a reverse bias of 250 V. The dopings of the epitaxial layer, and the substrate are taken to be 1×10^{15} cm^{-3} both. The peak doping in the channel which is assumed to be doped with a Gaussian profile is taken to be 10^{17} cm^{-3}. The n^+ type drain is assumed to be heavily doped.

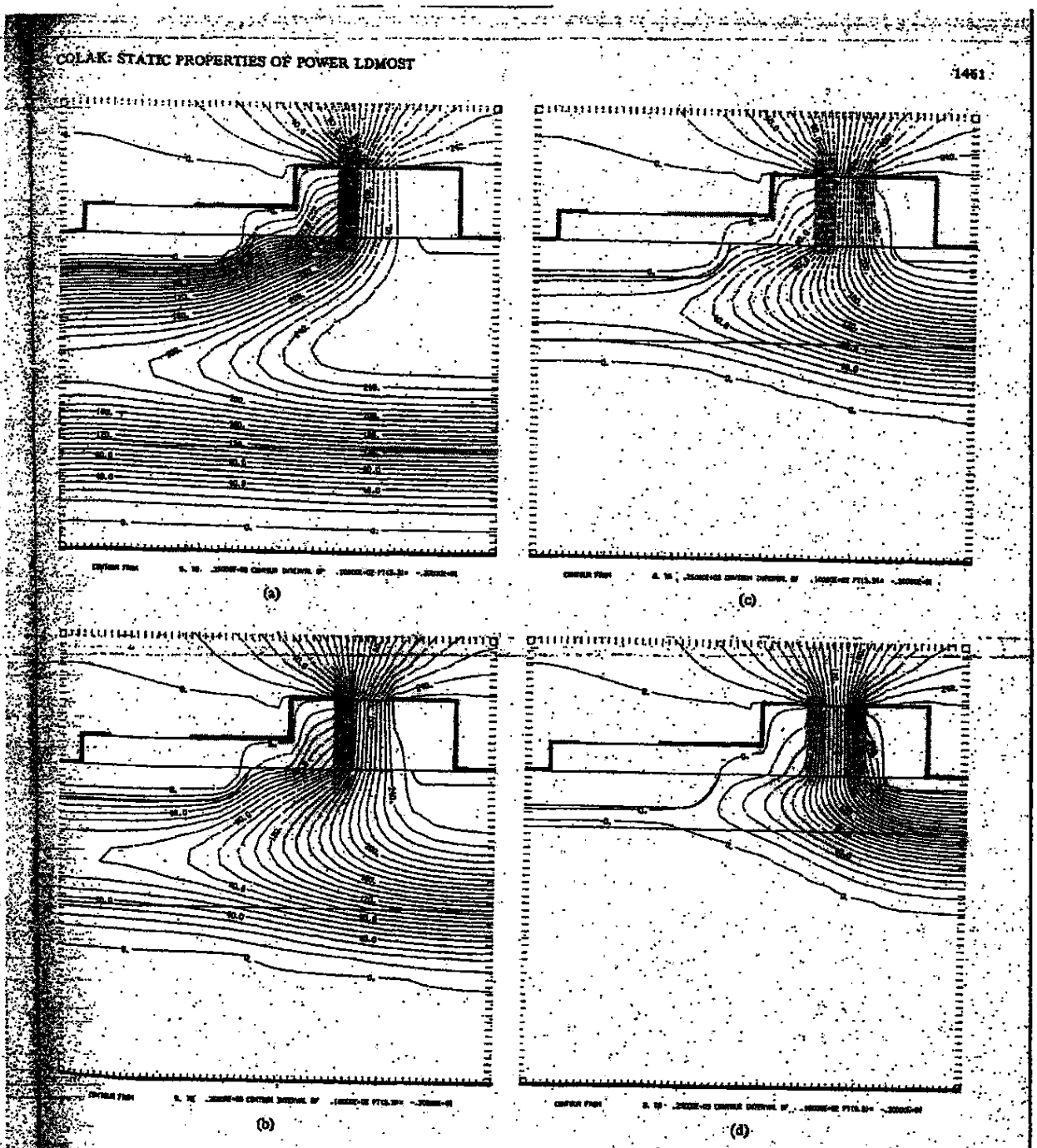


Fig. 11. The potential contours for the DMOST of Fig. 9 for different epitaxial layer thicknesses. (a) t_{epi} = 30 μm. (b) 20 μm. (c) 14 μm. (d) 8 μm. The doping levels are the same as given in Fig. 10, and the reverse bias applied is 250 V.

this study, it has been assumed that avalanche breakdown will occur whenever M_p and M_n are both greater than 2. As mentioned earlier, it has been found that the breakdown conditions can be improved for transistors using an epitaxial layer as a part of their active region by choosing a thin layer [12]. This can also be true for extended drain region configurations [25] obtained by an ion-implantation at the surface which acts like a pinched resistor. In these cases, the depletion region of the substrate becomes effective in shaping the contour lines in the region of the epitaxial layer near the channel. The effects of epi thickness are shown in Fig. 11. The potential distributions were calculated for four epi thicknesses. All other parameters held constant. The interaction between depletion layers in the channel and substrate regions is slight for

thick epitaxial layers (Fig. 11(a)). The fields then are high near the curved portion of the channel doping and also below the edge of the gate metal. As the thickness of the epitaxial layer is decreased (Fig. 11(b)), two depletion regions interact more strongly and, the potential lines become less crowded in high field areas, finally reaching a relatively uniform spacing (Fig. 11(c)). This is due to the reduction of the curvature effect and the spreading of the potential distribution between the channel and the drain. If the epitaxial layer is made too thin, however, then the fields near the drain contact diffusion and drain metal edge increases (Fig. 11(d)). The high fields appearing near the drain in this case can be decreased by increasing the separation between the channel and drain at the expense of an increase in the device area.

In addition to obtaining the potential contours for each epitaxial layer thickness, the analysis is used to calculate the maximum voltages which may be applied to the drain before reaching avalanche breakdown. These values are plotted against epitaxial layer thicknesses in Fig. 12 for two different substrate doping levels. There is an optimum thickness for a given epitaxial layer resistivity which maximizes the breakdown voltage of the LDMOST. This optimum value of epitaxial layer thickness shifts towards lower values as the substrate doping is decreased. This is simply due to the fact that the resurfing capacity of substrates decreases as their doping decreases. For a given breakdown voltage, the maximum allowable substrate doping level, therefore, should be used to minimize the on-resistance by using the least resistive epitaxial layer.

The breakdown voltage of a given LDMOST geometry cannot exceed the breakdown value of the epi-substrate junction directly beneath the drain contact. To find the limiting value of the substrate junction breakdown, computations are done for a geometry similar to the one given in Fig. 9 but with varying drift region length. The epitaxial layer thickness for these computations is kept constant at $t_{epi} = 15\ \mu m$, which is close to the optimum thickness for highest breakdown. The substrate doping is also kept constant at $1.5 \times 10^{15}/cm^3$, which is slightly higher than previous computations. The remaining parameters of the device are given in Fig. 13(a). This geometry and parameter also corresponds to the experimental devices which were fabricated with different drift region lengths. The breakdown voltage and the average longitudinal electric field $E_{AV} = V_{BR}/L_d$ at the surface is plotted in Fig. 13(b) as a function of drift region length L_d. For a given set of parameters, increasing the drift region length increases the breakdown voltage up to a constant value determined by the substrate junction breakdown. For these parameters, the breakdown is limited by this effect to 415 V when the drift region length is greater than about 30 μm. Below this value, the breakdown is limited by localized high field regions in the drift region.

The highest longitudinal field obtainable with the geometry of Fig. 13(a) is about 14 V/μm. This value is limited by the effects of the gate and drain metal edges extending over the epitaxial drift region excessively, causing field crowding near these edges. To avoid this problem, and to maximize the average longitudinal electric field, the extension of the metallizations over drift region should be decreased. There is a trade-off, however, because the on-resistance of the device increases with decreasing gate extension as seen in Fig. 5.

To show this, a geometry was modeled which differed from the one in Fig. 9 only in that the distance between drain and

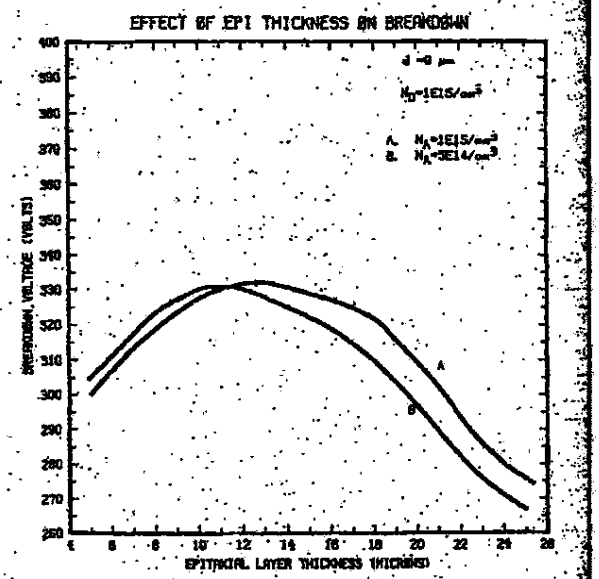


Fig. 12. The effect of the epitaxial layer thickness on the reverse breakdown voltage of DMOST given in Fig. 9 for two different substrate dopings, (A) $1 \times 10^{15}\ cm^{-3}$, (B) $5 \times 10^{14}\ cm^{-3}$. The epitaxial layer doping is $1 \times 10^{15}\ cm^{-3}$, and the separation between the gate and drain metals is $d = 9\ \mu m$.

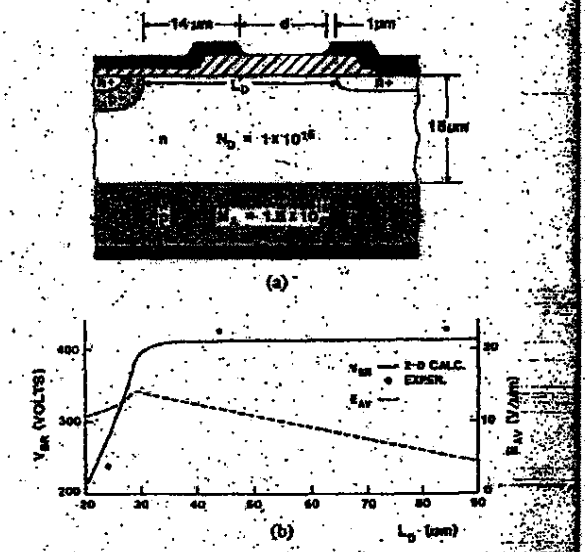


Fig. 13. (a) The geometry, and the parameters of the LDMOST for studying the effects of the net drift region length L_d' on breakdown. (b) The calculated breakdown voltage (solid line), and the average longitudinal electric field $E_{AV} = V_{BR}/L_d$ (dashed line), as a function of net drift region length $L_d' = L_d - L_b$. The discrete figures represent averaged experimental breakdown voltages measured.

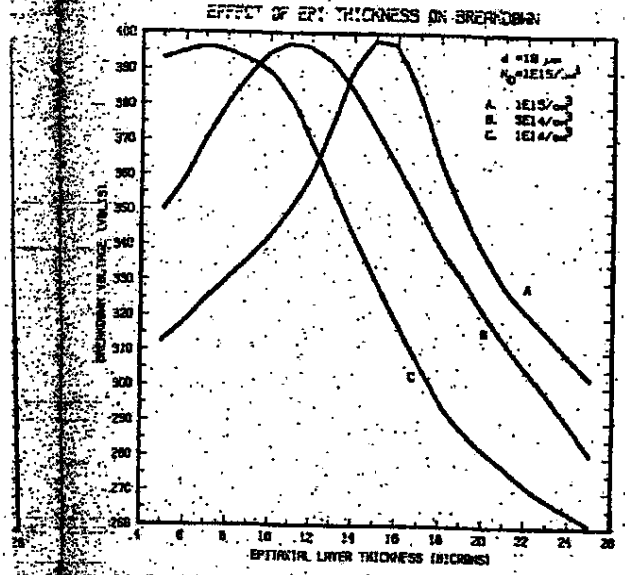


Fig. 14. Breakdown voltage as a function of epitaxial layer thickness for LDMOST with increased spacing between gate and drain metals $d = 18$ μm. The epitaxial doping level is 1×10^{15} cm^{-3}, and the substrate dopings are (*A*) 1×10^{15} cm^{-3}, (*B*) 5×10^{14} cm^{-3}, and (*C*) 1×10^{14} cm^{-3}. The remaining parameters are the same as given in Fig. 9.

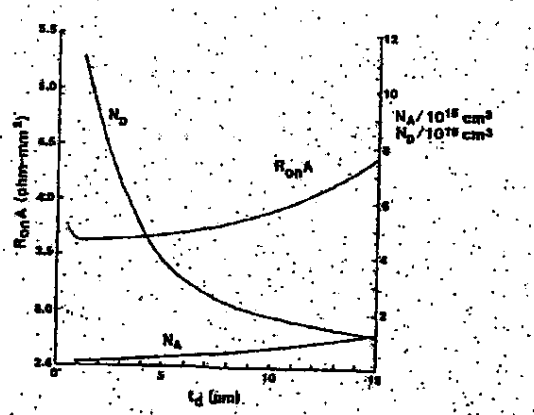


Fig. 15. Substrate and epitaxial layer doping levels, and the normalized on-resistance of a resurfed 400-V LDMOS transistor as a function of epitaxial layer thickness. The on-resistance values correspond to nearly optimized structures for the given breakdown voltage. The unit cell length is taken to be 50 μm. The necessary net drift region length "t_d" varies between 24 μm, and 27 μm depending on the epitaxial layer thickness.

gate metals was increased. The maximum breakdown voltage (Fig. 14) is now higher due to the reduced field crowding effects.

The maximum average longitudinal fields for the optimum epitaxial thickness for most designs modeled are between 15 V/μm and 20 V/μm, with lower maximum average fields at higher breakdown voltages. This indicates that resurfing the device permits one to use the silicon material close to its ideal intrinsic dielectric breakdown limit. Since the electric field in the well-designed device is essentially constant throughout the drift region, the breakdown voltages observed are higher than the one-dimensional ideal limit for the epitaxial material.

Another property of the resurfed LDMOS transistors is that the electric field at the channel junction is reduced substantially. This electric field is usually lower than the average longitudinal fields. This leads to a decreased depletion region penetration into the channel. The channel in thin-layer resurfed devices, therefore, can be made much shorter and with lower doping compared to conventional designs without causing punch-through breakdown. The frequency response of the device is also improved due to the smaller gate-to-channel capacitance achievable with the thin-layer LDMOST.

Design Optimization and Conclusions

The on-resistance model for LDMOST presented in this study takes into account the current spreading and saturation in the drift region. Good agreement has been found between the results of this model and experiment both in the unsaturated and saturated regions of the current. The dependence of the limiting on-resistance of the device on the various geometrical properties of the drift region has been studied in detail. The dependence of LDMOST breakdown voltage on the drift region properties has also been studied and these dependencies have been verified with experimental devices. Device design criteria to obtain the maximum breakdown are given. Combination of the models for the on-resistance and the breakdown allow for the optimization of the device geometry as explained in the following paragraph.

For a given breakdown voltage, there is a continuous set of epitaxial layer thickness and doping pairs. Any combination of epitaxial doping and thickness from this set will give the desired breakdown voltage. However, excessively thick epitaxial layers are not desired because of the limitations to on-resistance reduction. Thus the desired thickness should be chosen from the linear slope region of the $R_{on}Z$ versus t_d curves similar to the one given in Fig. 4. Too thin layers require the use of very high doping in the drift region to assure resurfing for the same breakdown voltage. But then, the reduced majority carrier mobility will be effective in increasing the on-resistance of the device.

Fig. 15 shows the results of an optimization study to get the lowest $R_{on}A$ for a constant breakdown voltage of 400 V. Two of the curves give the necessary epitaxial and substrate dopings to have resurfing. The resultant normalized on-resistance is also plotted as a function of epitaxial thickness. The dotted region is an added extension (not calculated) to show the functional dependence to be expected for extremely thin layers, and represent the area where mobility reduction due to high epitaxial doping increases the on-resistance. The on-resistance of a resurfed device is minimized by choosing the epitaxial layer thin so that current spreading becomes negligible. The information on the dimensions of the unit cell is given in the figure caption.

The use of this optimization analysis for the resurfed LDMOST devices results in a reduced channel to drain separation for a given breakdown voltage. The electric fields within

this separation approach the dielectric breakdown field of intrinsic silicon. The design approach presented permits the fabrication of LDMOST's which are comparable in size to the vertical technology devices. Further improvements in the performance of LDMOST are expected by using field shaping semiconductor layers [26] or by passivating the surface of the device by materials like SIPOS [27].

Appendix I
Conformal Mapping of Drift Region Geometry

The two-dimensional geometry of the drift region is shown schematically in Fig. 2. To be able to find its resistance, this region is first conformally mapped to a simpler geometry. For the present problem, the drift region geometry is transformed into a simple rectangle. The two opposite sides of this rectangle contain only the accumulation and drain contact regions which are shown as L_a and L_b, respectively, in Fig. 2. For this, the transformations between a rectangle and the half space [28] defined in Fig. 16 are used. In this transformation k^2 is the parameter and K is the real quarter period of the elliptic functions. The imaginary quarter period K' is defined by $K'/K = b/a$ and these quarter periods are related to the parameter by $1/k = Sn[(K + iK'), k^2]$.

The original drift region geometry and the mapped rectangle are shown in Fig. 17. For this type of mapping, three separate transformations are used which are given in Fig. 16. These are

$$W_1 = Sn^2\left(\frac{K}{L_d} z, k^2\right) \tag{12a}$$

$$W_2 = \left(\frac{1-\zeta}{\zeta}\right)\frac{W_1}{1-W_1} \tag{12b}$$

where

$$\zeta = Sn^2\left(\frac{K}{L_d} L_a, k^2\right) \tag{12c}$$

and

$$W_3 = \frac{U_1}{L} Sn^{-1}\left(\sqrt{W_2}, \zeta^2\right) \tag{12d}$$

where U_1 is the length of the final rectangle on the real axis, and L and ζ^2 are the real quarter period and the parameter, respectively, of the elliptic function for the final transformation. The resultant rectangle is shown in Fig. 17(b). Fig. 17(a) is the geometry of the drift region sketched upside down for algebraic simplicity. The transformations in (12) first map the geometry of Fig. 17(a) into a half plane (12a), then scale the real axis of this half plane (12b and 12c), and finally transform this scaled half plane back to another rectangle (12d) as shown in Fig. 17(b).

The solution of Laplace's equation in the rectangle of Fig. 17(b) is straightforward (Ohm's law) and gives $E_{\rho_3} = (V/U_2)\hat{p}_3$. The current is $I_{\rho_3} = (Z/\rho)\, U_1 E_{\rho_3}$. V is the applied potential, ρ is the resistivity of epitaxial material (taken directly because the transformation is a direct geometric transformation), and Z is the width of the device. The quantities U_2 and U_1 are geometric and have length dimensionality. From this the resistance of the drift region is found to have the form

$$R = \frac{V}{I} = \frac{\rho}{Z} f(L_d, t_d, L_a, L_b) \tag{13a}$$

where

$$f(L_d, t_d, L_a, L_b) = \frac{U_2}{U_1}. \tag{13b}$$

U_2 and U_1 are defined by $U_2/U_1 = L'/L$ where L' and L are the imaginary and real quarter periods of the elliptic functions used in the final transformation given in (12d).

U_2/U_1 ratio can be calculated exactly from the properties of elliptic functions by using only the geometrical parameters of the drift region. For thin layer devices, these calculations can be simplified by approximations and the U_2/U_1 ratio is given by [29].

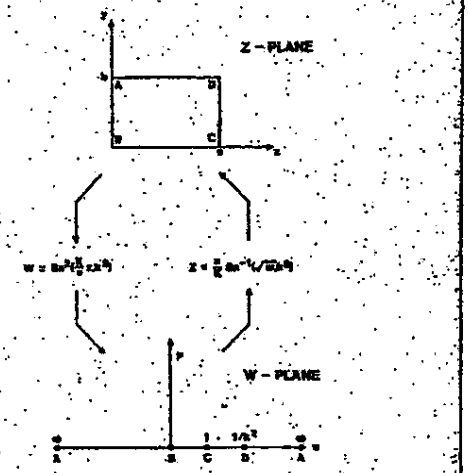


Fig. 16. Transformations between the inside of a rectangle in the Z-plane, and the upper half of the W-plane by using the Jacobi elliptic function $Sn(a, b)$.

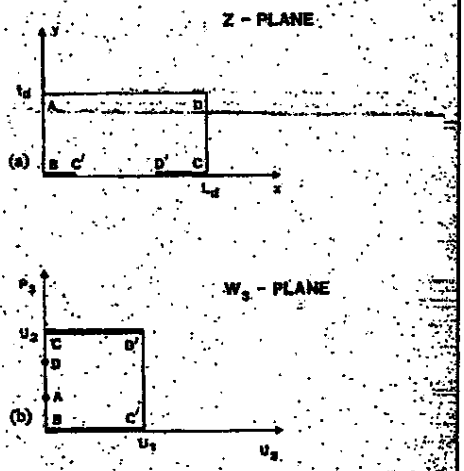


Fig. 17. (a) The simplified drift region geometry of LDMOST in the Z-plane. (b) The corresponding transformed rectangle in the W_3-plane.

$$\frac{U_2}{U_1} \simeq \frac{1}{\pi} \ln \frac{1}{(\zeta^2/16) + 8(\zeta^2/16)^2 + 84(\zeta^2/16)^3 + 992(\zeta^2/16)^4} \quad (14a)$$

This expression is valid for $\zeta^2 \leqq 0.16$ or $u_2/u_1 \geqq 1.5$. The parameter ζ^2 of the elliptic function used in the $W_2 \rightarrow W_3$ transformation is given by

$$\zeta^2 = \frac{\mathrm{sn}^2(\chi_1, k^2)}{1 - \mathrm{sn}^2(\chi_1, k^2)} \cdot \frac{1 - \mathrm{sn}^2(\chi_2, k^2)}{\mathrm{sn}^2(\chi_2, k^2)} \quad (14b)$$

where

$$\chi_1 = KL_d/L_d \quad (14c)$$

$$\chi_2 = K(L_d - L_o)/L_d \quad (14d)$$

$$k^2 \simeq 1 - 16 \exp\left[-\pi \frac{L_d}{t_d}\right] \quad (14e)$$

and

$$K \simeq 1.3863 + 0.11197(1 - k^2) + 0.07253(1 - k^2)^2 + [0.5 + 0.12135(1 - k^2) + 0.02888(1 - k^2)^2] \cdot \ln[1/(1 - k^2)]. \quad (14f)$$

The relations (14e) and (14f) are obtained from [29] and they are valid for $(L_d/t_d) \geqq 2.5$, or $(1 - k^2) \ll (1 - k^2)$. For the same range, however, the elliptic functions also have an approximate expression [29] which is given by

$$\mathrm{sn}(\chi, k^2) \simeq \tanh(\chi) + \frac{(1 - k^2)}{4} \cdot [\sinh(\chi)\cosh(\chi) - \chi]\,\mathrm{sech}^2(\chi) \quad (15)$$

Using the geometrical parameters of the drift region in (14), and (15) and substituting the results in (13) gives the value of the drift region on-resistance.

Appendix II
I-V Model for the Channel Region

LDMOST has a short and inhomogeneously doped channel. Thus the correct characterization of the channel requires a two-dimensional analysis taking these into account. However, the present study is done for biasing conditions for which the drift region parameters are the dominating factors in the overall device behavior. Thus a one-dimensional empirical model [5] is taken for the channel, keeping in mind that the errors introduced by this model will not affect the overall device characteristics very much. According to this model, the normalized channel current is given by

$$\frac{I_c}{Z} = \frac{\mu}{\ell} g(V_c, V_G) \quad (16a)$$

where

$$g(V_c, V_G) = C_{ox}\left\{\left(V_{GT} - 2\phi_{FP} - \frac{V_{ce}}{2}\right)V_{ce} - \frac{2}{3}\kappa\left[(V_{ce} + 2\phi_{FP})^{3/2} - 2\phi_{FP}^{3/2}\right]\right\} \quad (16b)$$

$$V_{ce} = V_c \quad \text{for} \quad V_c < V_{csat}$$
$$V_{csat} \quad \text{for} \quad V_c \geqq V_{csat}. \quad (16c)$$

C_{ox} is the oxide capacitance per unit area given by ϵ_{ox}/t_{ox}, where ϵ_{ox} and t_{ox} are the dielectric constant and the thickness of the oxide, μ is the effective mobility in the channel, and ℓ is the channel length. The mobility and channel length are modeled separately in the text.

The effective gate voltage is $V_{GT} = V_G - V_T$, where V_T is the threshold voltage of the channel given by

$$V_T = \phi_{MS} + 2\phi_{FP} - \frac{Q_{ss}}{C_{ox}} + \frac{\sqrt{4\epsilon_s q N_A \phi_{FP}}}{C_{ox}}. \quad (17)$$

ϕ_{MS} is the metal-to-silicon work function difference, ϕ_{FP} is the effective fermi potential in the channel, Q_{ss} is the surface state charge, N_A is the effective channel impurity concentration ($\simeq 1 \times 10^{15}$ for the present study), and ϵ_s is the silicon dielectric constant.

V_{csat} is the channel saturation voltage driven by [30]

$$V_{csat} = V_{cs} + \ell_0 E_m - \sqrt{V_{cs}^2 + (\ell_0 E_m)^2} \quad (18)$$

where ℓ_0 is the unmodulated channel length, E_m is the longitudinal electric field in the channel for velocity saturation. This empirical field value is taken to be 1×10^4 V/μm. V_{cs} is the channel pinchoff voltage given by

$$V_{cs} = V_{GT} - 2\phi_{FP} + \frac{\kappa^2}{2}\left[1 - \sqrt{1 + \frac{4V_{GT}}{\kappa^2}}\right] \quad (19a)$$

where

$$\kappa = \frac{\sqrt{2\epsilon_s q N_a}}{C_{ox}}. \quad (19b)$$

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High Efficiency Inversion Layer Solar Cells on Polycrystalline Silicon by the Application of Silicon Nitride

REINHOLD SCHÖRNER AND RUDOLF HEZEL

Abstract—Plasma enhanced CVD silicon nitride is introduced for the fabrication of inversion layer solar cells on p-type polycrystalline silicon. The same high interface quality as obtained for Si-nitride on monocrystalline silicon could also be achieved for polycrystalline silicon. This includes high interface charge densities up to 6.6×10^{12} cm^{-2} and high UV sensitivity of the cells. For 4-cm^2 polycrystalline metal-insulator-semiconductor inversion layer (MIS/IL) solar cells active area efficiencies up to 13.4 percent (12.3-percent total area efficiency) under AM1 illumination could be reached, the highest values yet reported for polycrystalline silicon inversion layer solar cells on a total area basis. For the coprocessed MIS/IL cells on monocrystalline 0.7-Ω · cm p-Si (100) under AM1 illumination active area efficiencies of 16.5 percent (14.4-percent total area efficiency) were obtained. For further characterization of the polycrystalline and of the monocrystalline cells, dark I-V curves, and I_{sc}-V_{oc} measurements at various illumination levels are presented.

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Introduction

RECENTLY it has been demonstrated that Si-nitride and Si-oxynitride represent attractive dielectrics for monocrystalline silicon metal-insulator-semiconductor inversion layer (MIS/IL) solar cells [1]–[3]. The unique properties of these films such as very high density of fixed positive interface charges to create a highly conductive inversion layer at the silicon surface, long term stability of these charges, low surface

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High Voltage MOS Integrated Circuits,
A Technology And Application Overview

Any generally useful high voltage MOS technology should be capable of implementing high performance low voltage functions.

Depending on the high voltage requirements, it seems to be relevant to distinquish between three different cases:

1. Open drain configuration
2. Transmit an output voltage e.g., push and pull
3. General case, the possibility to handle ± voltage

1. Open Drain

In this case, one does not have the high voltage on the chip, one gets it externally via a load resistor. Then, just the drain of the current sinking transistor has to withstand the high voltage. The transistor is generally operating with a grounded source, thus the transistors can be driven directly from the low voltage logic.

The technology to solve the open drain case has, so far, mainly been structured around conventional N-MOS, P-MOS and C-MOS technologys, where one can add ion implanted extended drain regions offset or stacked gates or lightly doped drain regions to achieve the high voltage output devices.

Exhibit I - Figure I shows the principal crossection for offset gate and lightly doped drain.

Exhibit II - Figure I shows a 400V device from NEC where they use an ion implanted extended drain region and a shielded source structure which prevents possible bipolar breakdown. The shielded source structure also implies a shorter extended drain region and thus makes a more efficient device.

As a figure of merit one uses ROA where RO in the resistance in the linear region and A is the active area.

The figure of merit for the NEC 400 volt transistor is about 50ohm mm2 to compare with 150ohm mm2 for a similar 400 volt transistors from Sharp (see Exhibit III - Figure I).

The highest voltage reported so far is 1000 volt (Tektronix, Exhibit IV - Figure I) using somewhat similar structures.

Using a D-MOS transistor and the resurf principle (an epi layer of opposite polarity, see Exhibit V - Figure 4) the current capability can be increased considerably. For a 400 volt device, Philip's has reported a figure at merit of around 6ohm mm2 which is six times improved compared to the NEC device.

But still the current capability is 2-3 times worse than for bipolar devices.

This has so far limited the applications to voltage ranges that cannot easily be handled by bipolar technology and where RO is not that critical.

Typical applications are for display driving in the 200-400 voltage range. Vendors for such devices are:

- Sharp
- Supertex
- Siliconix
- Telmos

Telmos is also marketing a C-MOS gate array with several open drain output transistors.

Recently, AMI and Holt have announced display drivers for vacuum fluorescant displays which are in the 30-50 volt range.

Thus the applications so far have been restricted to multiple output devices, if one on the other hand needs just one very high performance output transistor. One can use a substrate transistor with a performance similar to a discrete one. This was started out in bipolar technology, see Exhibit VI - Figure 2 and 4.

In Smartpower II Motorola uses a D-MOS verticle transistor in combination with C-MOS logic in a structure which is very similar to the Nationals.

Application areas for this high current high voltage devices are shown in Figure I. By the way, the Motorola Smartpower I device was developed especially for the automotive industry where there is a large need for high performance PNP drivers.

2. Voltage Transmitting Case

If one, for example, uses N-channel transistors in a push-pull configuration, both the source and the drain have to withstand the high voltage. For transmitting the high voltage through the pull up transistor, one needs the high voltage on the gate, this has to be created through some level shifting arrangements. The high voltage on the gate will require a thicker gate oxide than for the low voltage devices.

Exhibit VII - Figure II shows an example of how this can be realized using D-MOS transistors. For level shifting they use a bootsharp precharge technique, see Figure V. One generally needs a high voltage N-channel and P-channel transistor for effective level shifting. Another drawback using two N-channel transistors is that for high voltage, the pull-up transistor will have a higher threshold voltage from heavy back biassing which will be seen as a voltage drop between the source and the drain. A proposal from Xerox, Exhibit VIII - Figure I, seems then much more attractive. Here they use C-MOS where they have applied the extended drain concept for both the N-channel and P-channel device (Note: for C-MOS. just the drains for the two transistors and the, well of course, have to withstand the high voltage).

For the P-channel device, they further use the resurf principle e.g., the well under the drain should be well depleted before breakdown between drain and well. Furthermore, this is fully compatible with low voltage C-MOS logic, in fact they use the same well 5um deep both for high voltage and low voltage devices. In the paper, they report working devices up to 200 volt.

3. General Case, The Possiblity To Handle ± Voltage

Consider the proposal from Xerox again. Assume one put a negative voltage on the substrate, then their concept will no longer work as one will have punch through between the drain and the substrate for the P-channel device. Their concept with shallow well works as long one has the same potential on the drain and the well. To sustain a high negative voltage one should then need a very deep P-well. Siemens has reported a 26um deep well for sustaining 200 volt. By putting a negative voltage on the substrate, one further destroy the compability with low voltage C-MOS. Using P-MOS in an isolated N-well should then be the obvious choice, further one is restricted to use the rather bad extended drain transistors. From this and the superior performance of D-MOS transistors, the main choice, so far, to handle the general case has been either junction isolation or dieletric isolation.

Exhibit I - Figure II shows the principle structure in a junction isolated process where a lateral D-MOS transistor is used. a more effective solution should be to use a vertical D-MOS structure similar to the one which is used for discrete power D-MOS devices.

This approach has been taken by Thompson CSF, Exhibit IX - Figure 2, on a 7ohm em 20um thick epi 200 volts drain-source breakdown voltage has been achieved, they use this for an Integrated Video Amplifier. In the same structure, the breakdown voltage for a bipolar NPN transistor should be below 100 volt. So this is then an improvement in voltage capability by a factor of two. Note that they also use the inherent bipolar transistors in the structure. To use them, if they can handle two voltage, seems to be the general case as they still are more area effective then the D-MOS transistor.

For example, Texas Instrument in their BIDFET technology uses a combination of D-MOS, bipolars NPN and JFETS, and C-MOS for low voltage logic. This technology they use for SLIC and display drivers.

200 volt has generally been considered as a practical limit for junction isolation, due to the thick epi and following deep isolation diffusion.

In the lower voltage range ≤ 100 volt which can be handled by the bipolar technology, a popular approach seems to be to combine low voltage C-MOS with the bipolar high voltage transistors. Companies using this include at least Motorola, Analog Devices, Sprauge and Unitrode, also, probably PMI.

An interesting approach to further extend the voltage limit for a junction isolated process, has been to use a lateral D-MOS device together with the resurf principle.

Exhibit X - Figure II shows a proposal from Philips.

Exhibit XI - Figure II shows a proposal from Motorola.

They both use very similar resistivity and epi thickness as in the Thompson case. They report making devices up to 300 volt so composed to the Thompson approach, they gain another 100 volt. Furthermore, these lateral devices are probably at least as area efficient as the vertical D-MOS one. To obtain still higher voltages, one seems to have to go to dielectic isolation. Bell has reported about a 400 volt switch for subscribes line interface, see Exhibit XII - Figure II. To realize the P-channel device for low voltage logic, they just merge the bases of two D-MOS transistors together. Harris uses a similar technology for the SLIC. Recently, also Telmos has developed a dielectic isolated process.

4. Conclusion

High voltage MOS integrated circuits in open drain configuration has so far mainly found applications for display driving in the voltage range 200-300 volt where existing bipolar technology can not handle it. The alternative choice is to use discrete transistors.

However, rapid progress in C-MOS compatible logic, (in the 2-3 um range, C-MOS has the same speed performance as TTL-LS and a higher packing density) and a general trend to wish to integrate more logic will sure make it to find more applications.

The rather large area output devices will then not hurt seriously as in many cases the chip area will be dominated by the logic functions. The output devices will sure also be improved.

For the voltage transmitting case about the same as above, may be true. However, in this case, the large area extended drain transistors may hurt more and it seems not so easy to apply the more effective resurf devices.

In certain cases it might be more effective to use an isolated technology.

For the ability to handle both + and - high voltage, resurf devices have extended the practical operating limit from 200 to 300 volt. The practical limit for the epi thickness has so far considered to be around 20um which sure can be somewhat extended to reach 400-500 volts for junction isolation.

Exhibit I

ity because of high fields across gate oxides, very thick epitaxial layers and their consequent isolation problems, and because of parasitic bulk and surface devices. Practical junction isolated circuits appear to be limited to about 200 volts. Dielectric isolation techniques will improve this figure because all of the above problems are eliminated by this technology except the need in transmission gate type applications for high gate oxide fields.

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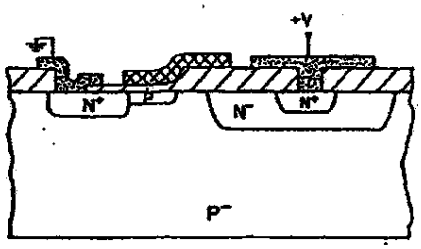

Fig. 1. Schematic cross-section of a high voltage output MOS transistor compatible with low voltage NMOS or DMOS circuits.

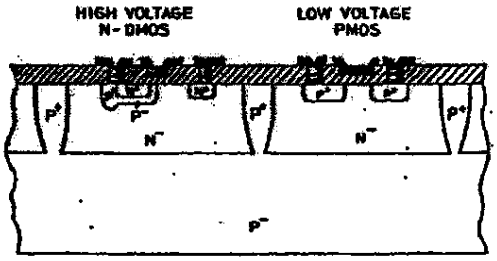

Fig. 2. Cross-section of general purpose high voltage technology based upon thick epitaxial layers and lateral DMOS devices.

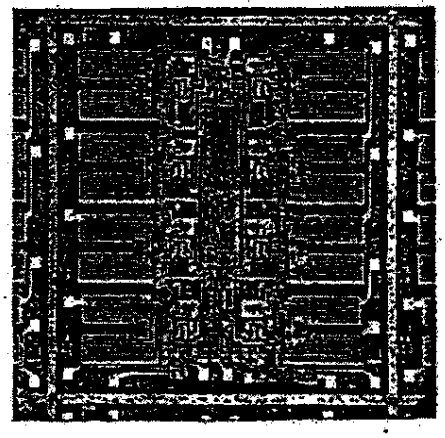

Fig. 3. Photomicrograph of integrated circuit fabricated with the technology of Fig. 2.

Exhibit II.

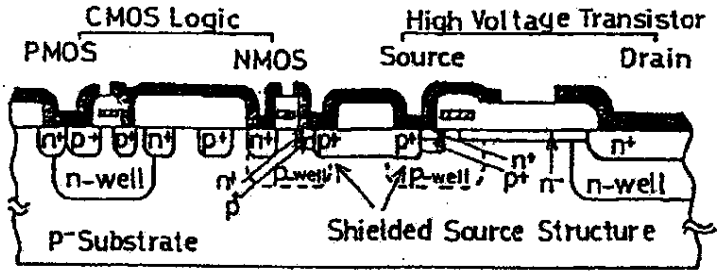

Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper n⁺ source layer entirely shielded by a lower p⁺ ground layer.

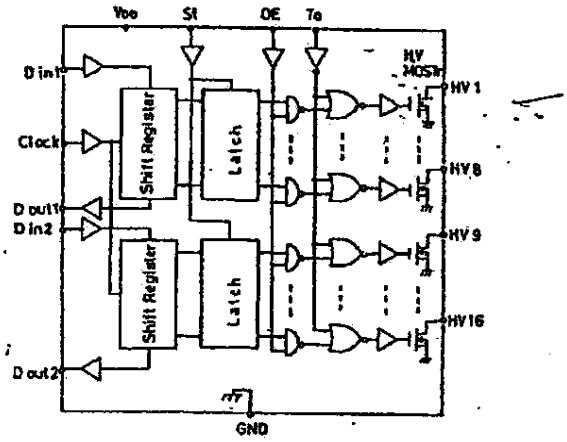

Fig.2 16 output high voltage MOS IC blockdiagram. Logic circuit is composed of serial-in and parallel-out shift registers, latches, gates and buffers.

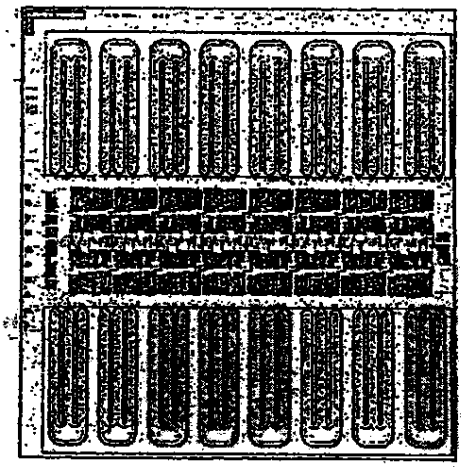

Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

V_B = 400V

R_{on} = 30Ω

I_{DS} = 0.5A

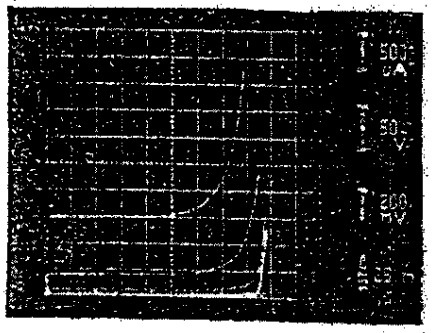

Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

Exhibit III

SESSION III: SOLID-STATE DEVICES

WAM 3.6: 400V MOS IC for EL Display

Katsumasa Fujii, Yasuo Torimaru, Kiyotoshi Nakagawa, Takeo Fujimoto and Yoshimasa Aoki

Sharp Corp.

Nara, Japan

A NUMBER of MOS developments have been attempted to provide operation at voltages higher than 200V[1-5]. Among these, DSA[6] MOST seems to have a promising future. This paper will describe a high voltage, DSA MOS IC which operates in excess of 400V. It was designed as a driver for electroluminescent displays[7]. Low voltage logic and thirty-two high-voltage output transistors are integrated on a single chip. The device consists of a pair of layers patterned as concentric conductive annular strips above which a layer of metal with a circular gap is deposited. This configuration and final passivation over the metal layer permit encapsulation in a plastic package. The high voltage DSA MOST was proposed earlier with a π substrate, a Diffusion-Self-Aligned structure, lightly doped drift region(N^-), and a field plate extended from the drain electrode[1]. The drift region of this device was not covered by field plates; i.e., an offset gate structure. If the field plate is extended to cover all of the drift region in these devices, the elect ic field at the edge of the drift region will be enhanced and the breakdown voltage reduced.

Figure 1 shows a cutway view of high-voltage DSA MOST and Figure 2 the $V_D - I_D$ characteristics. The main feature of the device is that the drift region is, as a whole, covered by multilayer field plates which consist of two conductive plates extending from the drain and source electrodes, and double-layered floating plates. Because a multiplicity of these floating field plates reduces the electric field enhancement, the structure does little to affect the high voltage characteristics of the offset gate MOST. The offset gate MOST should be hermetically encapsulated to prevent degradation of the device characteristics affected by moisture and/or ionic contamination. The lifetime on-resistance increase by 10% at various temperatures in earlier devices is shown in Figure 3; a comparison between hermetic seal and plastic packages is also indicated. Though the lifetime of the hermetically sealed device is longer than that of the plastic-packaged device by a factor of six, its reliability is poor.

Results of bias aging are shown in Figure 4. The changes of R_{ON} and I_{DS} in the device characteristics are small and the breakdown voltages at V_{GS} = 5V (duty cycle = 0.1%) always exceed 400V. The plastic-packaged device surpassed the results of earlier packaged devices; Figure 3. The plastic-packaged device has some advantages; for example, its cost could be made low and the discharge between a bonding wire and the die edge is eliminated.

High-voltage monolithic integrated circuits for electroluminescent graphic display drivers have also been designed. A block diagram and photomicrograph of a 32b high-voltage MOS IC are shown in Figures 5 and 6, respectively. The logic circuits contain a 32b serial-in/parallel-out shift register, latch and gate circuits. They can operate at a single +5V power supply, and the data I/O interface is TTL compatible. The high-voltage MOST gates are directly controlled by an STB input and $\overline{CL}$ input, even when the shift register is transferring the data.

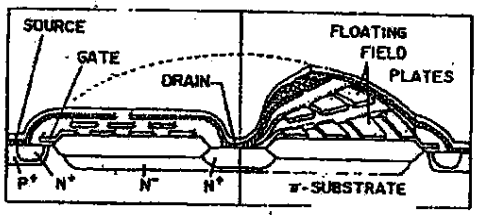

FIGURE 1—Cutway view of the DSA MOSFET.

High Voltage MOSFET	
Drain-Source Breakdown Voltage	400V
ON-Drain Current	50mA
Drain-Source ON Resistance	500Ω
Logic Circuit	
Supply Voltage	+5V
I/O Interface	TTL Compatible
Clock Frequency	dc to 10MHz
Technology	DSA E/D MOS
Chip Size	5.76mm x 3.44mm
Package	42 pin DIP

TABLE 1—Typical characteristics of 32b high-voltage MOS IC.

*Based on concepts of S. A. Arrhenius.

[1] Awane, K. et al., "High-Voltage DSA-MOS Transistor for Electroluminescent Display," *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 224-225; Feb., 1978.

[2] Cohen, R. W. et al., "A High-Performance Planar Power MOSFET," *IEEE Trans. Elec. Dev.*, Vol. ED-27, No. 2, p. 340-343; 1980.

[3] Temple, V. A. et al., "A 600V MOSFET Designed for Low On-Resistance," *IEEE Trans. Elec. Dev.*, Vol. ED-27, No. 2, p. 343-349; 1980.

[4] Sakuma, H. et al., "A High Voltage Offset-Gate SOS/MOS Transistor," *IEDM Digest of Technical Papers*, p. 594-597; 1979.

[5] Okabe, T. et al., "A Complementary Pair of Planar-Power MOSFETs," *IEEE Trans. Elec. Dev.*, Vol. ED-27, No. 2, p. 334-339; 1980.

[6] Tarui, Y. et al., "Diffusion Self-Aligned Enhance-Depletion MOS-IC," *Proc. 2nd Conf. on Solid State Devices, Tokyo*, p. 193-198; 1970.

[7] Takeda, M. et al., "Practical Application Technologies of Thin-Film Electroluminescent Panels," *SID Int. Symposium, Digest of Technical Papers*, p. 66-67; Apr.-May, 1980.

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Mrs. H. Eklund
Exhibit 4

PROCESS AND DEVICE DESIGN OF A 1000-VOLT MOS IC

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ABSTRACT

High-voltage MOS devices and NMOS logic circuits have been integrated on the same chip by using a silicon-gate isoplanar process that is compatible with present NMOS-LSI technology. The electrical characteristics of a high-voltage MOS device are modeled and characterized in terms of channel length, drift-layer length, drift-layer ion dose, and extended-source field-plate effect. The device structure and the process parameters are optimized to obtain maximum drain saturation current with a low on-resistance and a drain breakdown of 1000 volts. The optimized high-voltage MOS device can perform at a saturation drain current as high as 84 mA with on-resistance as low as 300 Ω within an area of 520 μm × 1320 μm while maintaining a drain breakdown of 1000 volts and drain leakage current less than 30 nA.

INTRODUCTION

High-voltage MOS integrated circuits are becoming important as driver devices in various display and switching applications. In order to integrate high-voltage MOS devices and logic circuits on the same chip, two different basic approaches have been demonstrated: one uses a vertical MOS structure (1), the other uses a horizontal structure (2-4). In this paper, the authors describe an advanced high-voltage MOS-IC technology that uses a horizontal device structure with a silicon-gate isoplanar process that is compatible with present NMOS-LSI technology. The device structure and the process parameters are optimized to provide a 1000-volt drain-breakdown voltage with maximum drain saturation current and minimum on-resistance.

DEVICE STRUCTURE AND MODEL

Figure 1(a) shows the cross-section of the high-voltage MOS IC. The high-voltage MOS devices are integrated with NMOS logic circuits on the same chip by using a silicon-gate isoplanar process. The gate electrode of the high-voltage MOS device is driven directly by the output signal of the logic circuit. The high-voltage MOS device has an enclosed structure with an extended-source field plate. Because a recessed-oxide technology is employed in the high-voltage MOS device, the channel region is self aligned not only with the source region but also with the drift-layer region, which in turn is self aligned with the drain region. The logic circuit consists of conventional silicon-gate enhancement- and depletion-mode MOS devices.

Figure 2 shows the schematic model of the high-voltage MOS device. The drain current first increases almost linearly with the drain voltage. The on-resistance is composed of channel resistance and drift-layer resistance. In the case of the race-track pattern shown in Fig. 1(b), the drift-layer resistance R_d is given by

$$R_d = \left[\frac{2\pi q \mu_d N_d}{\ln(1 + L_d/R_D)} + \frac{2q\mu_d N_d W_p}{L_d}\right]^{-1}. \quad (1)$$

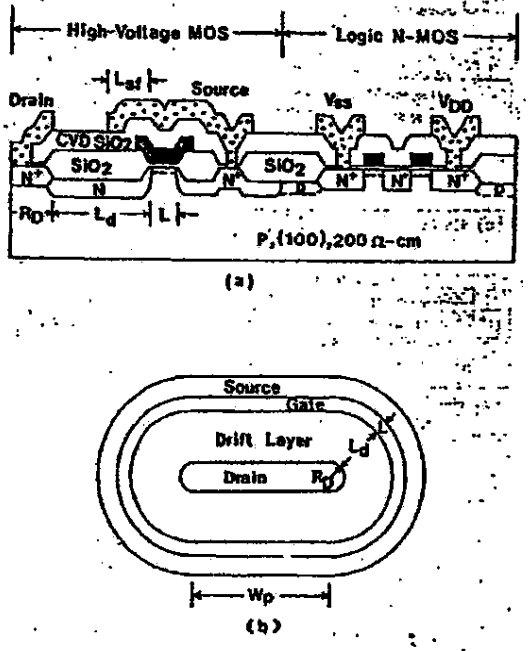

Figure 1. (a) High-voltage MOS-IC device structure. (b) High-voltage MOS device pattern.

where N_d represents the total mobile-carrier density in the drift layer. If it is assumed that the drift layer has a uniform impurity distribution and is reverse biased by a drain voltage V_{DS} and a substrate voltage V_{SB}, then N_d is given by

$$N_d = N_{d0} - \frac{N_{d0}}{X_{jd}}\left[\frac{2\epsilon_{si}(V_{DS} + V_{SB})}{q}\frac{N_{SB}X_{jd}}{N_{d0}}\frac{1}{(N_{SB} + N_{d0}/X_{jd})}\right]^{1/2}. \quad (2)$$

where N_{d0} is the total ion dose implanted into the drift layer and X_{jd} is the junction depth of the drift layer. As the drain voltage is increased, the channel region close to the drift layer (p_1) is pinched off as shown in Fig. 2(b).

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Exhibit V

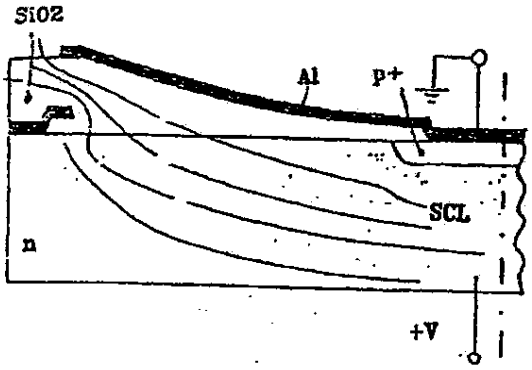


Fig. 1 Basic planar p–n junction using field plate

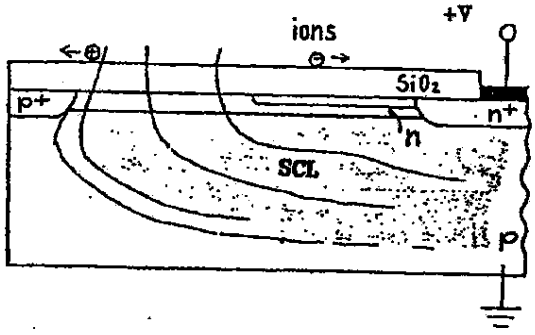


Fig. 3 "Resurf" junction termination

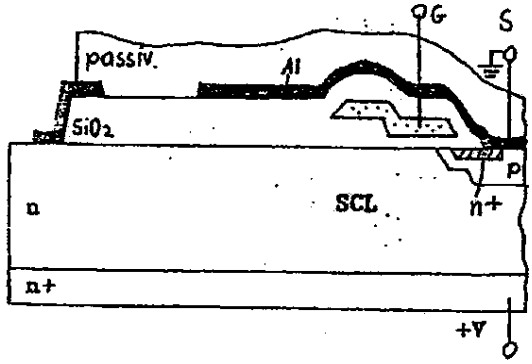


Fig. 2 Junction termination of a V DIMOS FET

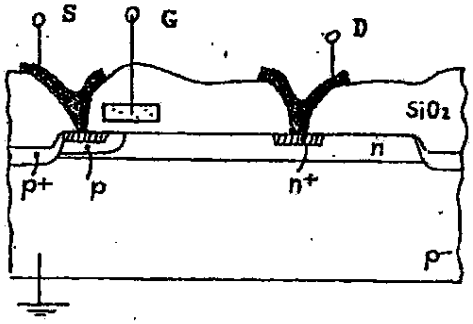


Fig. 4 Resurf-based lateral HV MOSFET

The other method of surface field reduction is the "Resurf" principle (1) shown in its simplest form in Fig. 3. The heavily doped region is surrounded by a lightly doped surface layer, which terminates in a heavily doped region of the substrate. The weakly doped surface layer depletes, compensating for the substrate space charge under reverse bias and causing a forced lateral extension of the surface space charge region. As a result, the surface field becomes virtually constant, having only small peaks at the two ends of the lightly doped zone.

The Resurf principle, although compatible with most IC processes, particularly those using ion implantation, is used mainly for lateral HV MOS devices. Different implementations exist which deviate slightly from the basic structure, as illustrated in Fig. 4.

INTEGRATED DEVICES

Two main groups of ICs can be distinguished in the integration of HV structures.

The HV ICs integrate generally low voltage logic and HV output stages on a single chip. They are devoted mainly display driving and telephone IC applications where the essential performance factor is high voltage capability.

The other group contains chips with integrated low voltage input circuit or functionally integrated structures.

These devices are used to switch really high power and are supported by additional functions to achieve superior performance.

HV ICs

The HV ICs can be classified according to the isolation techniques used.

Junction isolation is the oldest isolation form and has been used widely by bipolar IC producers. A novel version working at up to 200 V has been in-

Exhibit U.
Exhibit U

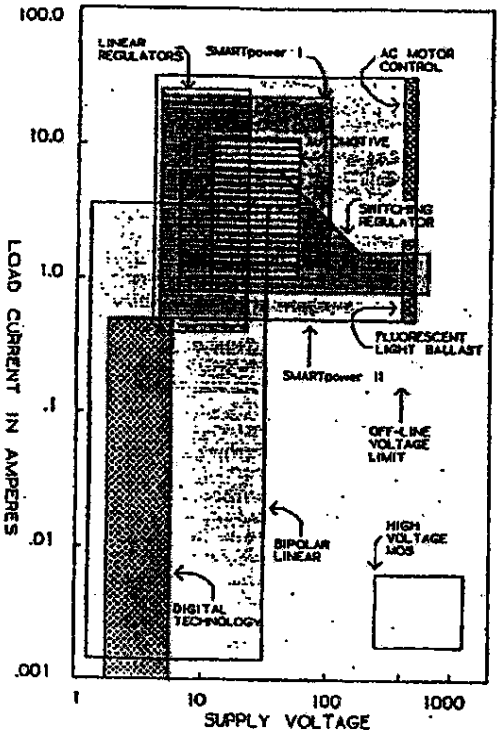


Figure 1. Capability and market overlap for power IC technology.

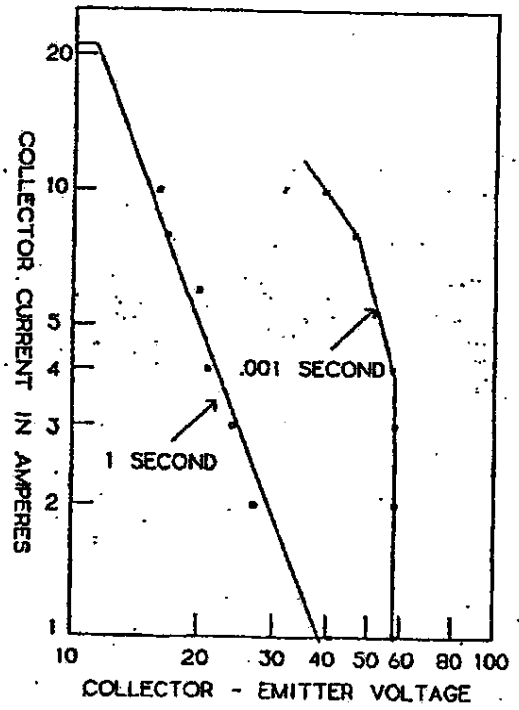


Figure 3. SOA curve of the SMARTpower I PNP output transistor.

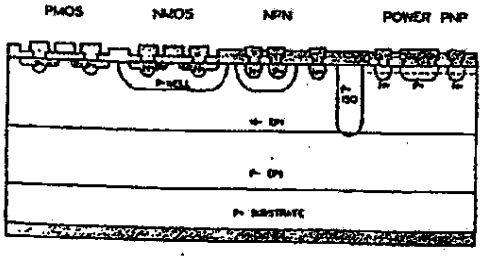


Figure 2. SMARTpower I device cross section.

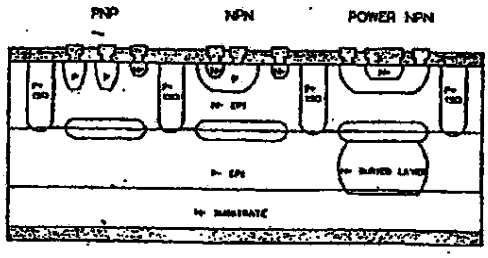


Figure 4. Cross section of the National bipolar STEEL technology (11).

Motorola

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-15, NO. 3, JUNE 1980

Exhibit VII

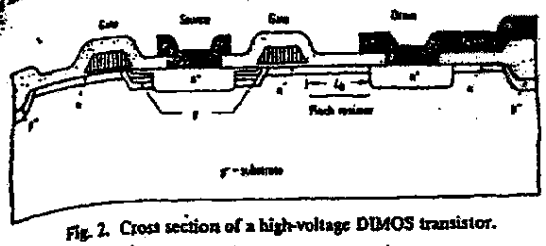
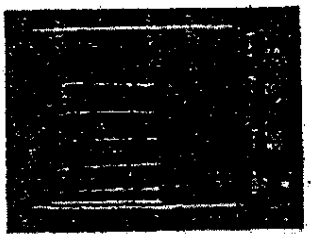
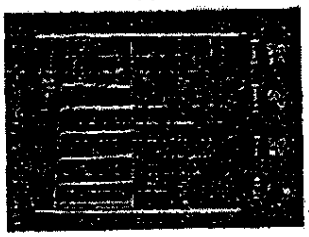


Fig. 2. Cross section of a high-voltage DIMOS transistor.



(a)



(b)

Fig. 3. Current-voltage characteristics of high-voltage transistors: (a) $L_D = 12\ \mu m$; $BV_{DS} > 100$ V; (b) $L_D = 30\ \mu m$; $BV_{DS} > 200$ V.

occurs. A 30 μm-test device can handle more than 200 V [Fig. 3(b)]. With higher substrate resistivities, for example 50 Ω · cm, breakdown voltage is improved to about 300 V. Compared with DMOS the DIMOS device shows a different punch-through behavior. The reason is that the p-doped DIMOS channel with its relative high concentration surrounds the n⁺-source region only in lateral, but not in vertical (bulk) direction (Fig. 2). Thus at low substrate dopings punch-through can occur earlier than in DMOS devices. Therefore a more sophisticated layout of DIMOS devices must be employed.

Another important point to consider in circuit design is the bulk effect. If these transistors are used in a high-voltage push-pull configuration, the pull-up device suffers severely from an increasing threshold voltage.

Fig. 4 shows the threshold voltage behavior at high substrate bias voltages. Four typical curves are plotted in this diagram. Parameters are the substrate resistivity with 20, 50, and 80 Ω · cm and the boron implantation dose for the DIMOS channel with 2 and 2.5×10^{12} cm^{-2}, respectively. These curves show, that for operating voltages in the range of 100 V and more, a substrate resistivity of more than 50 Ω · cm should be used. Then an efficient circuit operation with threshold voltage below 2.5 V seems to be possible.

High-Voltage Output Buffer

The first design was the well-known single-stage output buffer circuit with a bootstrap push-pull configuration [5], shown in Fig. 5.

The high-voltage devices—T_1, T_2, and T_3—are necessary,

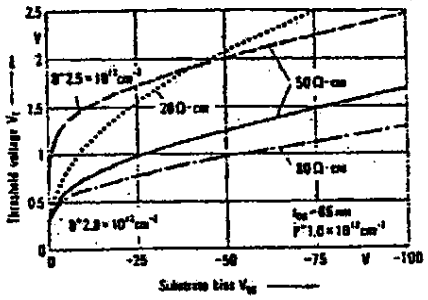


Fig. 4. Threshold voltage (V_T) behavior at high substrate bias voltages V_{BS}. Parameters: substrate resistivity; boron dose of the DIMOS channel implantation.

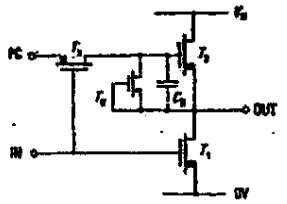


Fig. 5. Circuit diagram of the single-stage output buffer circuit.

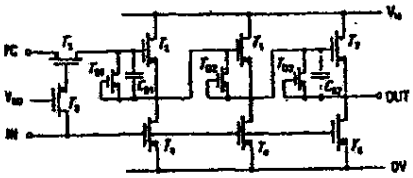


Fig. 6. Circuit diagram of the three-stage output buffer circuit.

T_D. This device is designed as a low-voltage transistor with a breakdown voltage below 25 V, which prevents the pull-up device T_2 from a gate oxide breakdown.

For a pull-up operation, first the bootstrap capacitor C_B is charged via the switched-on transfer device T_3 with the precharge signal *PC* going "high." When the slightly delayed (~20 ns) input signal *IN* goes "low," T_3 is switched off. Thus the gate of the pull-up device T_2 is isolated and can be bootstrapped to a voltage level well above V_H.

The circuit must be able to operate with 5 V input and precharge levels. To achieve both high switching speed and low power dissipation, the following provisions should be made.

1) High-voltage dc paths to ground are not allowed. Therefore usual level shifters cannot be used.

2) The precharge time should be minimal.

3) The effective gate voltage of the pull-up device should be large enough to compensate for stray capacitors—and the bulk effect.

The last point cannot be accomplished by this circuit. Therefore it suffers from a large rise time at higher supply voltages. Applying 50 V rise times of more than 1 μs have been measured. A better solution is a three-stage output buffer design shown in Fig. 6. The first stage is constructed similarly to the single-stage circuit. The additional transistor T_8 effects a bootstrapping of the gate of the transfer device T_3. Thus the full supply voltage level V_{DD} is applied to the bootstrap capacitor C_{B1} during precharge. The second stage with T_4 and T_5 serves as buffer between the first stage and the bootstrap

Exhibit VIII

In re U Ehlund

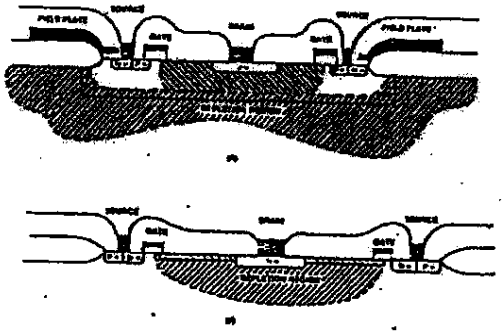


Figure 1. (a) High voltage p-channel structure; (b) High voltage n-channel structure.

wafers are oxidized. An Si_3N_4 film is deposited and patterned, followed by patterning and implanting with boron for the channel stop areas. A thick oxide is grown selectively in the field area. Then the Si_3N_4 film and the initial oxide underneath is removed and the gate oxide of 1000 Å thick is grown. The threshold voltage of the n-channel transistors is adjusted by patterning and implanting boron in the gate areas. The polysilicon film is deposited, doped, patterned and etched. The p-type offset channel is formed by implanting boron followed by patterning and implanting phosphorus for the n-type offset channel. The heavily doped P^+-source and drain areas are formed by implanting BF_2 into photoresist patterned wafers. Then the thin oxide film is grown to protect implanted areas and the new photoresist pattern is printed and etched for the N^+ source and drain. The N^+ areas are formed either by As-implant or by outdiffusion from the phosphorus rich CVD SiO_2 film which is deposited and reflowed at high temperature. Contacts are etched and the interconnections are formed by patterning an Al film. The protective phosphorus-doped SiO_2 film is deposited and pad areas are defined.

EXPERIMENTAL RESULTS

In this series of the experiments for the development of the integrated high- and low-voltage CMOS transistors the shallow well concept was verified. Although the reported results are satisfactory for the purpose for which they have been developed, it is expected that higher breakdown voltages can be achieved by further optimizing the process parameters.

The typical drain characteristics of the high-voltage n-channel transistors are shown in Figure 2. The drain breakdown voltage at zero biased gate is in excess of 400V, exhibiting almost linear dependence on the offset channel length. The drain leakage current is less than 1 nA. The typical characteristics of the p-channel transistors are shown in Figure 3, when the drain is connected to the substrate and the source is connected to the field plate. The drain breakdown voltage is over 225V, and the drain leakage current is less than 1 nA at zero gate bias voltage. The well-to-substrate breakdown voltage is in excess of 400V for the 30-micron wide field plate. Both high-voltage transistors are stable at high temperature. Punch-through between source and drain is not observed for channel gate lengths as small as 8 microns.

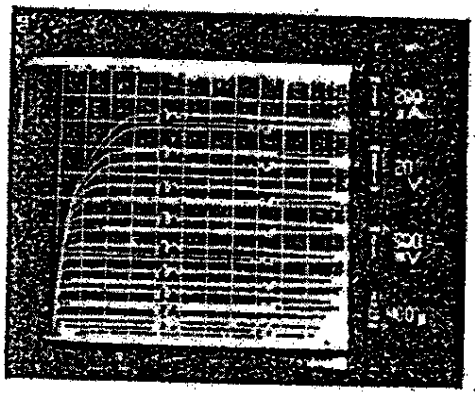


Figure 2. Typical drain characteristics of high-voltage p-channel device with the offset channel 40 microns long.

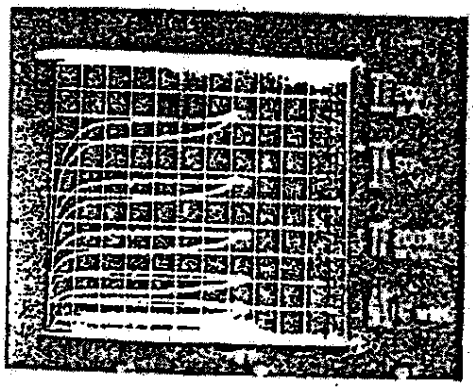


Figure 3. Typical drain characteristics of high-voltage n-channel device with the offset channel 70 microns long.

Exhibit IX

SESSION II: CONSUMER CIRCUITS

WAM 2.3: Integrated High-Voltage Video Amplifier for Color TV

Bernard DesCamps and Jean-Claude Rufray

Thomson CSF Semiconductor Division

Saint-Egreve, France

THE COLOR TV cathodic tube is driven by a high voltage, wide-band, low switching time dc amplifier. Hybrid and discrete amplifiers are used in present TV receivers. The integration of this function requires a high voltage capability for the circuit to obtain correct output signal dc level (brightness) and dynamic range (contrast). The presence of high voltage in an integrated circuit can induce parasitic channels in the silicon and a multilayer technology is therefore used to make metal field shields. The high voltage devices are N-channel DMOS which have better breakdown voltage characteristics than in the bipolar transistor counterparts and which, in addition, do not present the second breakdown phenomenon[1].

A video amplifier for one color channel is shown in Figure 1(*a*). In the IC there are basic elements: input differential amplifier with bipolar transistors (T_4, T_5), cascode amplifier with DMOS (T_1) and current driver with DMOS (T_2, T_3).

The gain of the video amplifier is externally adjusted by a series resistance in the input; (Figure 1(*b*)). The feedback resistance is connected between the input and the output. This gain adjustment is necessary to compensate for the gain difference between each color tube gun. The circuit contains a minimum number of components to obtain a low cost product.

The circuit output is connected to a 15pF capacitance (tube and wiring). This capacitance must be charged and discharged by a 100V supply in 150ns. The DMOS transistors T2 and T3 are designed to give 12mA with a 10V gate supply. To obtain the required risetime at the output, the T2 gate-drain capacitance must be charged at the same speed.

The gate-drain capacitance is 2.5pF, and therefore resistor R1 can be lower than 80kΩ. A 50kΩ value has been chosen. The dynamic range is calculated by the product of R1 and II of the current generator (4mA). The high-voltage DMOS transistor structure is shown in Figure 2. The vertical DMOS was chosen over the lateral DMOS because its structure permits one to reach a higher breakdown voltage[2]. This breakdown voltage is improved by limiting the electric field at the channel-drain junction periphery.

The technology is an adaptation of a classical IC bipolar technology to obtain high voltage capability[3]. Circuit components are junction isolated. High isolation breakdown voltage results from the choice of: the substrate resistivity (14–20Ω-cm), the depth of the diffused buried layer, the epitaxy characteristics (7Ωcm, 20μ).

To help isolate the 20μ thick epitaxial layer, P^+ foundations are implanted before epitaxial growth. DMOS fabrication requires the introduction of additional steps to classical bipolar fabrication to provide self-alignment of the P channel and the N^+ diffusion, channel implantation, and gate oxide layer.

The two aluminum interconnection layers are isolated by a composite nitride oxide layer. The first interconnection layer is used for the electric field shields and the DMOS gate. This metalization layer has sloped edges to help insure a good step coverage of the second aluminum layer.

The electrical characteristics of the integrated VDMOS appear in Figure 3. A 200V drain-source breakdown voltage has been achieved. The circuit shown in Figure 1 has been processed on a 3x2mm² chip. Figure 4 is a photomicrograph of the integrated circuit which contains three video amplifiers. The main specifications are given in Table 1. The total IC power dissipation in the worst case (white picture) is lower than 3W. For the other cases the total system dissipation is the same, but a part of the power is dissipated in the feedback resistances. With a 230V dc supply the output signal which can be obtained is shown in Figure 5.

The dc voltage (black level) is 120V. The dynamic range is 140V. The risetime is 150ns for 100V peak-to-peak.

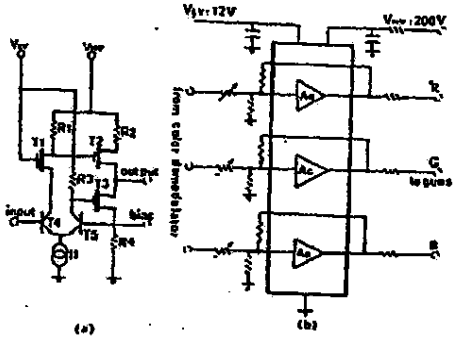


FIGURE 1—Circuitry contained in each amplifier (*a*); block diagram (*b*).

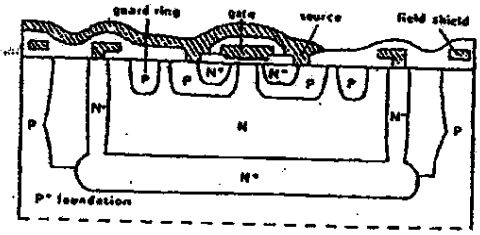


FIGURE 2—DMOS structure.

[1] Plummer, J. D. and Meindl, J. D., "A Monolithic 200V CMOS Analog Switch," *IEEE J. of Solid State Circuits* — Vol. SC 11, No. 6; Dec., 1976.

[2] Krishna, S., "Second Breakdown in High Voltage MOS Transistors," *Solid State Electronics*, Vol. 20; 1977.

[3] DesCamps, B., "A Compatible DMOS Bipolar Technology Analog IC," *ESSDERC 78*; DGRST Contract No. 77.7.0986.

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Exhibit X

HIGH-VOLTAGE DMOS AND PMOS IN ANALOG IC'S

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Philips Research Laboratories
Eindhoven - The Netherlands

ABSTRACT

A lateral 300V DMOS device is described which can be integrated in a standard bipolar IC process. The device, applicable as a high voltage source follower for analog circuits, is based upon the "double-acting resurf" principle; a modification with an interrupted p- top layer or with a stepped field plate is used. The p- layer improves the interconnection-induced breakdown and can be used in the extended drain of a 280 V PMOST.

INTRODUCTION

For functions like driving transducers or CRT's and for analog switches, high voltage analog stages of over 250 V may be needed on the chip. Vertical bipolars are less suitable because of the required thick epi-layers and even integration of vertical DMOS devices in a standard IC process is rather difficult. High voltage lateral MOS devices of over 500 V, using thin layer extended drain or "resurf" techniques (1-3), can easily be incorporated, but a high voltage source follower is impossible. Source followers using lateral DMOS devices and 25-30 µm epi have been reported (4); here 200 V is considered the limit for junction isolated devices because of deep isolation diffusions and parasitic bulk and surface effects (5). Recently a "double-acting resurf" technique has been reported (6); compared to "resurf" as mentioned above, it not only offers better lateral conduction but also prevention of substrate punch-through in follower applications. Owing to a higher doping content of the n layer (about 2.10^{12} cm^{-2}), the depletion layer at source (back gate)-to-substrate breakdown does not extend to the surface diffusion (as shown by the left-hand shaded area in fig. 1) and no punch-through occurs. At high voltage on the n^+ drain with the other terminals grounded, a high field would occur at the source edge. By using a p-top layer, depletion of the n layer is obtained from the top and the bottom (right-hand shaded areas in fig. 1) causing a

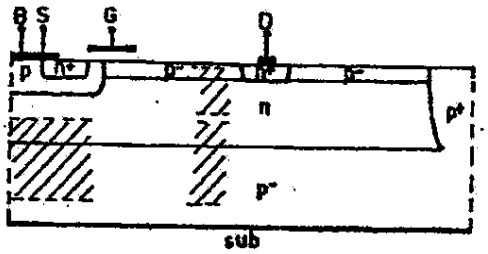

Fig.1. A double-acting resurf structure.

smooth voltage decrease over the lateral distance between source and drain; at high drain voltage this p- top layer has to be depleted too. The effect was demonstrated on JFET and lateral bipolar devices (6); the p_s and n layers were optimized at 0.5 10^{12} cm^{-2} and 1.8 10^{12} cm^{-2} respectively.

LATERAL DMOST

For proper functioning of a lateral DMOST (LDMOST), the design of fig. 1 has to be adapted. In fig. 2 a window is shown, made locally in the p-layer at the source side; electrons from the gate-controlled surface channel now pass through a vertical JFET which limits the current capability and increases the on-resistance. The window dimensions are therefore a compromise between on-resistance and breakdown.

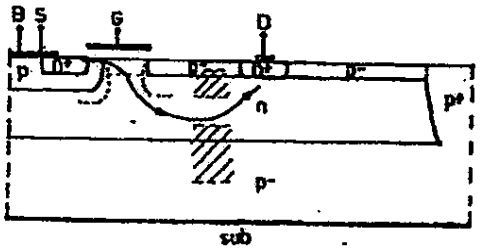

Fig.2. LDMOST with interrupted p-layer.

0-7803-1832-5/82/0000-0081 $00.75 © 1982 IEEE

Exhibit 81

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DEVICE	BV_{CEO}	BV_{CBO}	VPT_{BS}	BV_{DSS}
NPN/DMOS WITH BURIED LAYER	52	136	200	100
NPN/DMOS WITH NO BURIED LAYER	250	320	160	330
NPN/DMOS NPN WITH MODIFIED BURIED LAYER *	UNDER STUDY	310	200	330

* 5μM UNDERSIZE OF BASE (OR P-TUB) DIFFUSION

TABLE I
EFFECT OF BURIED LAYER - DMOS/BIPOLAR

Substrate	10 Ω-cm	(111)
Buried Layer	20 Ω/□	8 μm
Epitaxy	5 Ω-cm	15 μm
Isolation	5 Ω/□	18 μm
Deep Collector	4 Ω/□	14 μm
P-Tub *	300 Ω/□	5.0 μm
Base	125 Ω/□	3.0 μm
Emitter	5 Ω/□	2.0 μm
Gate Oxide *	-	100 nm
Pre-Ohmic	-	-
Metallization	-	150 nm
Final Passivation	-	500 nm

* Added Steps

TABLE II
PROCESS PARAMETERS

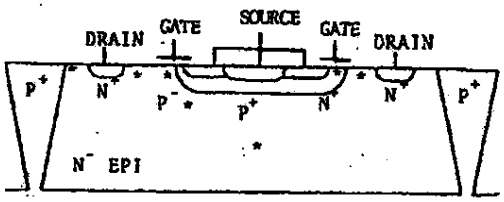


FIG. 1
POTENTIAL BREAKDOWN SITES
IN A LDMOS TRANSISTOR

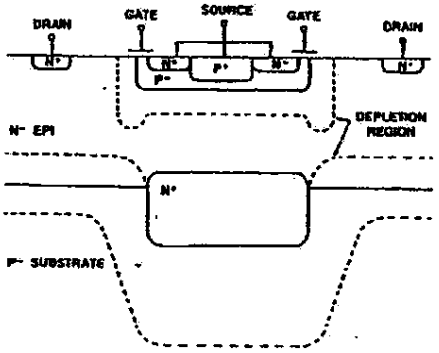
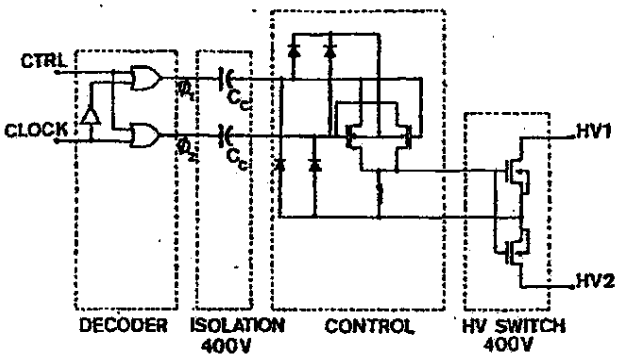
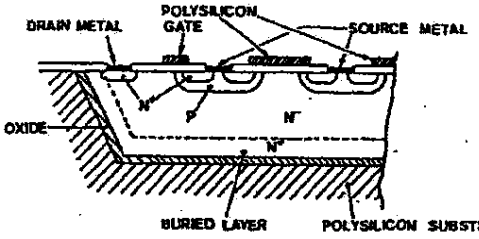


FIG. 2
GATE UNDERLAID LDMOS
TRANSISTOR

Exhibit XII





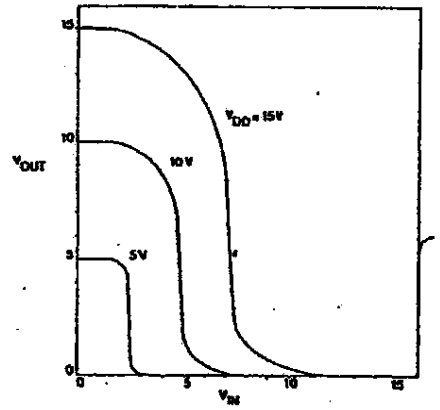


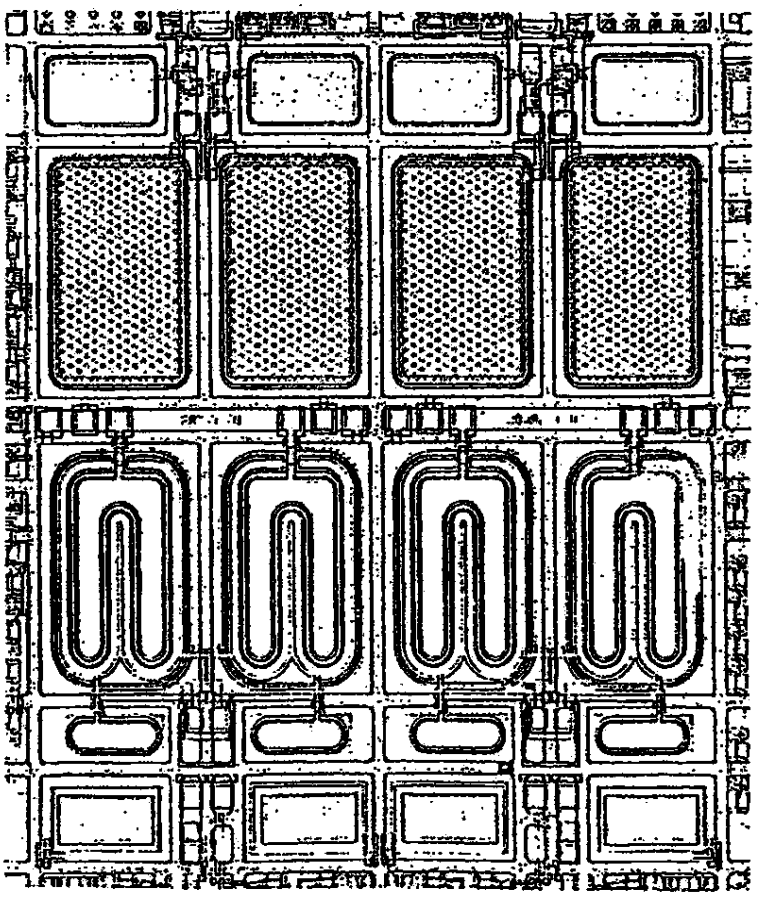
FIGURE 4—Transfer characteristics of a D-CMOS inverter gate for supply voltages VDD = 5V, 10V, 15V.

[Left]

FIGURE 2—Cross section of the DMOS transistor in a dielectrically-isolated bucket.

[Below]

FIGURE 5—Chip photo. Active area 5.0x5.6mm^2.



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DX 629

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DX 633

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